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PGEC Student Activities and Education in Computers*

H. H. GOODE†

LATE in 1953 the Professional Group on Electronic Computers initiated activities concerned with student relations. Recently the Student Relations Committee of the PGEC was established to foster these activities. The purpose of the Committee is to bring the PGEC to the attention of the students. To hold this attention after it has been gained, the Committee provides to students information on educational activities, professional meetings, technical advances and new applications; all relative to electronic computers. This program is presently being carried out by representatives of the Committee in the various chapters of the PGEC.

In 1953 when the effort in this field was starting, information was needed concerning the whereabouts of educational facilities in computers and computing. In order to obtain this information, a survey of educational activities in computers was undertaken. By-product objectives included: (1) the listing of faculty members whose interests were in computers so that they might represent the efforts of the PGEC at their respective schools; and (2) the designation of student representatives.

A questionnaire was distributed to all likely schools throughout the country. The response was excellent and in return for the attention to the questionnaire, the information was tabulated and the results sent to all those answering. The interest in the survey results was so marked that it was decided to keep the information up-to-date and to distribute the survey to school representatives at irregular intervals. Apparently the survey is useful beyond its original purpose. It provides: (1) an up-to-date summary of the present status of computer education; (2) a method of monitoring the growth of educational work; (3) for undergraduates interested in computers a source of information which helps them to select a proper place to do graduate work; (4) as well as a listing of interested persons who may be contacted concerning computing at various schools. It is our thought that because of these supplementary interests, the survey table will be of interest to readers of the TRANSACTIONS OF THE IRE.

Of the 155 schools contacted by questionnaire, 34 schools did not answer. Of the remaining 121, 31 had no facilities or computer courses. However, all of these latter provided the names of a faculty member most

* Original manuscript received, March 12, 1955.
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TABLE I

Column No.	Column Heading	Interpretation
1	University	
2	Graduate or Undergraduate	G—The institution has a graduate school. U—The institution offers only undergraduate courses.
3	Faculty Member, Title and Department	Name, rank, and position of person most interested in electronic computation, to whom information may be sent, and from whom up-to-date information may be obtained.
4 5 6	Orientation Design Operation	A program of courses in orientation, design, and operation is offered in A—*Analog* electronic computation. D—*Digital* electronic computation. 1—Projected Course: No program is currently available but one is planned or is under consideration. 2—Partial Course: Offerings in allied fields devote time to some aspects of electronic computation. 3—Existing Course: A program specifically designed for electronic computation is offered.
7	Facility	Facilities and equipment for performing: A—*Analog* electronic computation, or D—*Digital* electronic computation. 1—Are planned, ordered, or under construction, but not ready for operation. 2—Exist in the form of Special Purpose computers, or punched card machinery. 3—Exist in the form of Special Purpose computers; or punched card machinery, and a General Purpose computer is planned or under consideration. 4—Exist in the form of General Purpose computers.
8	Thesis	An asterisk indicates that suitable subjects on electronic computation are accepted for theses leading to advanced degrees.
9	Assistantships	An asterisk indicates that assistantships are available in the field of electronic computation.
10	Degree	An asterisk indicates that advanced degrees are granted in the field of electronic computation.
11	Seminar	An asterisk indicates that seminars in electronic computation are held regularly.

interested and 8 of the 31 provided a student representative as well. (Canadian institutions are recent additions to the survey. Being few in number they are not treated separately.) The 90 schools reporting facilities or courses appear in the table.

The key to the columns of the electronic computation education summary in Table II is shown in Table I.

With the designation of Student Committee Chairmen for each of the eleven chapters of the IRE PGEC the work of the Student Relations Committee is stabilizing at a productive level. The programs of these chapters include the provision of speakers and demonstration material for student meetings, encouragement of student membership in IRE and special affiliation with the PGEC, encouragement towards student papers and problem-solving in the field of computing, and the contribution of articles on computing to the IRE Student Quarterly. Further, the National Administrative Committee of the PGEC is considering the desirability of establishing fellowships in computing.

Because the field is growing so rapidly, and because almost all of the educational aspects of the field are relatively new, we may expect the picture of both the educational activity and the programs of the various sections to change rapidly. When these changes appear significant future reports will reflect them.

TABLE II

ELECTRONIC COMPUTATION EDUCATION SUMMARY[1]

1	2	3		4		5		6		7		8	9	10	11
University	Graduate or Undergraduate	Faculty Member	Title and Department	Orientation		Design		Operation		Facility		Thesis	Assistantship	Degree	Seminar
				A	D	A	D	A	D	A	D				
Akron	U	Sibila, K. F.	Prof., Head, EE	2	2	2	2	2	2	1		*			
Alabama Poly.	G	Summer, H. M.	Asst. Prof., EE				2								
Arizona	G	Russel, P. E.	Prof., EE			3	3			4		*		*	
Arkansas	G	Barnette, N. H.	Prof., Head, EE							4		*	*		
Brooklyn Poly.	G	Hebbert, C. M.	Prof.	3	3	3	3			4	3				
Brown	U	Angulo, C. M.	Prof.				2								
Calif., Berkeley	G	Morton, P. L.	Prof., Head, EE			3	3	3	3	4	3	*	*		
Calif., L. A.	G	Tompkins, C. B.	Head, CL		3				3		4	*	*	*	*
Calif., L. A.	U, G	Rogers, T. A.	Prof., Eng.	3	3		3			4	4	*		*	
Calif. Tech.	G	McCann, G. D.	Prof., EE					3	3	4	2				
Carnegie	G	Woodford, J. B.	Asst. Prof., EE	3	3	2	2	2	2	2		*			
Case Tech.	U	Brammer, F. E.	Prof.					3	2						
City College N.Y.	U	Taub, H.	Prof., EE			3	3								
Clarkson	U	Salerno, J.	Asst. Prof., EE	2	2										
Columbia	G	Zadeh, L. A.	Prof.			3	3	3	3		4				
Connecticut	G	Lof, J. L. C.		3	3			2		4					
Cornell	G	Credle	Prof.	3	3						3				
Dartmouth	G	Curtis, H. W.	Prof.	2	2			2		2					
Denver	U	Webb, R. C.	Prof., EE	1	1	3	3								
Detroit	G	Ahlquist, R. W.	Prof., Head, EE			2		2							
Drexel	U	Lange, E. O.	Prof., EE									*			
Georgia Tech.	U	Drucker, B. M.	Asst. Prof., MA	1	1	3	3	1	1	3	3				*
Geo. Wash.	G	Winter, R. E.					3				2				
Harvard	G	Aiken, H.	Head, CL	3	3	3	3	3	3		4				
Idaho	U	Hattrup, H. E.	Prof., Head, EE			2		3							*
Illinois	G	Nash, J. P.	Prof., MA				3		3	4	4	*	*		*
Illinois Tech.	U	Shien, S.	MA						3	3					
Iowa State	U	Boast, W. B.						3							
Kansas	G	Chai, Y.	Prof., Head, EE					3		4					
Kansas State	G	Wolfe, J. E.	Assoc. Prof., EE			2	3	1		4	4	*	*		
Kentucky	G	Smith, G. E.	Prof., EE						2						
Lafayette	U	Smith, F. W.	Prof., EE												*
Louisiana State	G	Ramsey, A. K.	Assoc. Prof.				2			1					
Louisville	G	Fife, S. T.	Prof., EE			2									
Maryland	G	Schulman, J. R.					2								
Massachusetts	U	Brown, R. R.	Prof., Head, EE	1		2		2		1					

[1] Compiled by the IRE-PGEC.

TABLE II (Continued)

1	2	3		4		5		6		7		8	9	10	11
University	Graduate or Undergraduate	Faculty Member	Title and Department	Orientation		Design		Operation		Facility		Thesis	Assistantship	Degree	Seminar
				A	D	A	D	A	D	A	D				
Michigan	G	Goode, H. H.	Prof., EE			3	3	3	3	4	4				*
Michigan State	G	Peterson, W. C.	Prof., EE			2	2			4					
Michigan Tech.	U	Sermon, T. C.	Prof., Head, PH							1					
Minnesota	G	Hess, P. N.	EE					3	3						
Miss. State		McKee, J. C.	Assoc. Prof., EE	3	1	3		3		4		*			
Mass. Inst. Tech.	G	Adams, C. W.	Asst. Prof., EE	3	3	3	3	3	3	4	4	*	*	*	*
Missouri	G	Vredenburgh, E. J.	Prof.					1							
Missouri Mines	G	Skitek, G. G.	Prof., EE									*			
Montana Mines	U	Schultz, F.	Prof., PH						2						
Nevada	G	Demers, M.	Asst. Prof., MA			2	2								
New York Univ.	G	Smith, J. S.				3	3		3		4				
Newark Engrg.	G	Dickey, D. W.	Asst. Prof., EE	3	3		2								
No. Car. State	U	Cell, J. W.	Prof., MA					2		4		*			
Northeastern	U	Essigmann, M.	Prof., EE				3		3						
Northwestern	G	Calvert, J. F.	Prof., Head, EE			2		3		4		*			
Notre Dame	U	Gorro, M. A.						1							
Ohio State		Cosgriff, R. L.	Asst. Prof., EE			3		3	1	4	2				
Ohio Univ.	U	Quisenberry, R. C.	EE			2									
Oklahoma	G	Lewis, W. B.	Asst. Prof.	1	1										
Oklahoma	G	Johnson, D. L.	Asst. Prof., EE				3					*			
Oregon State	G	Stone, L. N.	Assoc. Prof., EE					3	3	4					*
Pennsylvania	G	Rubinoff, M.	Asst. Prof., EE	3	3	3	3	3	3	1	1	*	*	*	
Penn. State		Warfield, J. N.	Director, CL			3	3	3		4	1	*	*	*	
Princeton	U	Surber, W. H., Jr.	Assoc. Prof., EE	3	3					4	2	*			*
Purdue	G	Ward, J. B.	Assoc. Prof., EE	3	3			1	3	4	4				*
Rennsselaer	G	Stoker, W. C.	Head, CL	1	1						1	*			
Rhode Island	U	Haas, R. S.	Prof., EE				2								
Rice	U	Pfeiffer, P. E.	Asst. Prof., EE	2		1		1	3	1		*			
Rochester	U	Dawson, C. H.	Assoc. Prof., EE						3						
Rutgers	G	Fender, F. B.	Prof., MA						3						
St. Louis	U	Buder, E. E.				3	3	3	3						
So. Dak. State	U	Cheadle, J. N.	Assoc. Prof., EE			2									
Stevens	U	Newman, E. G.				3	3								
Tennessee	U	Tillman, J. D.	Prof., EE			1	1		1		4				
Texas	U	Straiton, A. W.	Prof., EE	3	1										
Texas A. & M.	U	Rode, N. F.	Prof., EE	1	1			1	1	4	2	*	*		*
Tulane	U	Cronvich, J. A.	Prof.												*
U. S. Navy P.G.	G	Cotton, M. L.	Prof., EE	3	3	2	2	2	2	4	4	*			
Utah	G	Stephenson, R. E.		3	3										
Utah State	U	Cole, Larry S.	Prof., Head, EE	3	3										
Virginia Poly.	U	Barnes, G. C., Jr.	Prof., EE	3	2	3		3		1					
Washington	G	Eastman, A. V.	Prof., EE					2	3						
Wash. St. Louis	G	Koopman, R. J. W.	Head, EE					3							
Wash. State	U	Hacker, S. G.	Prof., MA						2						
Wayne	U	Jacobson, A.	Head, CL	3	3	3	3	3	3	4	4		*	*	
West Virginia	G	Keener, E. L.	Asst. Prof.			2									
Wisconsin	G	Rideout, V. C.	Assoc. Prof., EE	3	1	3	1	3	1	4	3	*	*	*	
Worcester	G	Kennedy, O. W.	Asst. Prof., EE	3		3		3		4		*			
Yale	U	Ordung, P. F.	Assoc. Prof., EE			2									
Canadian															
Alberta	G	Harle, J. A.	Prof., EE									*	*	*	
British Col.	G	Bohn, E. V.	Asst. Prof., EE	2		2				1		*	*		
Laval	G	Boulet, L.	Head, EE	2	2					1		*	*	*	
New Brunswick	G	Dineen, J. O.	Head, EE	2	2			2				*			
Toronto	G	Gotlieb, C. C.	Asst. Prof., PH		3				4			*	*	*	*
West Ontario	G	Nichools, R. W.	Asst. Prof., PH							2		*		*	

A Survey of Electronic Analog Computer Installations*

L. B. WADEL† AND A. W. WORTHAM†

Summary—A survey has been made of real-time electronic analog computer (differential analyzer) installations. This survey was conducted (1) so that a directory of the installations could be compiled and (2) so that various data regarding the installations could be made available for analysis. The survey was conducted by a mail questionnaire. Information was obtained regarding size of installation, size of staff, weekly usage of the equipment, age of installation, and availability to outside organizations from 96 installations having a total of 8,320 computer amplifiers. The results of the survey have been analyzed and are presented in this paper, together with the directory.

Introduction

THE Dallas-Fort Worth Chapter of the IRE Professional Group on Electronic Computers has conducted a survey of the United States and Canadian real-time analog computer installations. Questionnaires were mailed to 130 organizations which were thought to have such facilities; 96 questionnaires were returned and have served as a basis for the enclosed analysis. The questionnaires sought the following data:

1. Name of organization.
2. Address of organization.
3. Person in charge of computer.
4. Size of installation as measured by the number of computing amplifiers.
5. Size of technical staff associated with the computer.
6. Average number of operating hours per week.
7. Availability of the computer to outside organizations.
8. Date of the establishment of the computer installation.

Analysis of the addresses and organizations' names yielded the by-products of geographic data and the classification as to industrial, governmental, or university organization. The questionnaires were mailed during the period October, 1954–January, 1955. The resultant directory, plots, and tables have been termed the "1955 edition." It is hoped that future editions will be prepared which will be more nearly complete and even more informative.

Discussion of Terms

All of the terms used in the survey are self-explanatory with the exception of installation size. In order to define an index which describes adequately the computer size, an understanding of the electronic analog computer and its capability is necessary. The electronic analog computer (electronic differential analyzer) is a convenient tool for the design and analysis of dynamic systems, large or small, linear or nonlinear, electrical, electronic, mechanical, aerodynamic, pneumatic, chemical, economic, biological, or any combination.[1,2] This type of computer can be used simply to solve the differential equations describing a system, or it can be integrated with other components to simulate a larger system.

The key to the electronic analog computer's operation is the dc operational or computing amplifier. Such amplifiers perform the basic functions of summation, sign-changing, and integration, as well as other more specialized operations. Although utility of the computer depends also upon supporting equipment such as potentiometers, multipliers, and output recorders, the number of computing amplifiers provides the most convenient index to the capabilities of the computer. A given problem may take more or less amplifiers, depending upon to what extent passive networks are employed and how much flexibility in making parameter changes is provided for. Two simple examples are: (1) linear system described by a second-order differential equation, 3 amplifiers; (2) linearized longitudinal motion of an aircraft, perhaps 10 amplifiers. The fact that some problems require several hundred amplifiers is an indication of the complexity of today's technology, and of the electronic analog computer's abilities. It is for these reasons that the number of amplifiers was taken as the index of size for an installation.

Results and Discussion

A deadline was established so that prompt analysis of the questionnaires could be begun; it was necessary to process the data when 87 of the questionnaires (representing 7,866 amplifiers) had been received. However, all 96 installations reported are included in the directory. The numerical results are presented in tabular and graphical form below.

Geographic distribution of installations and amplifiers is shown in Table I, on the facing page.

Further analysis of the data shows that the average installation contains 90 amplifiers; is staffed by six

* Original manuscript received, February 11, 1955.
† Chance Vought Aircraft, Inc., Dallas, Tex.

[1] C. A. Meneley and C. D. Morrill, "Application of electronic differential analyzers to engineering problems," PROC. IRE, vol. 41, pp. 1487–1496; October, 1953.
[2] G. A. Korn and T. M. Korn, "Electronic Analog Computers," McGraw-Hill Book Co., Inc., New York, N. Y.; 1952.

ersons; is operated 39 hours per week; and was estab-shed in 1952. A detailed breakdown of the number of nstallations and the number of amplifiers in govern-nental (G), industrial (I), and university (U) (including rivate research institutes) service is presented in Table I for each availability classification: not available to utside organizations (N), available for use by govern-nent contractors (AG), and available (A).

TABLE I

Regions*	Number of Installations	Number of Amplifiers
Pacific	26	2981
Mountain	5	584
West North Central	5	398
West South Central	5	398
East South Central	2	50
East North Central	11	669
South Atlantic	6	404
Middle Atlantic	22	1832
New England	4	516
Canada	1	34
Total	87	7866

* U. S. Census Bureau, "Statistical Abstract of the United States: 953," (74th ed.), Washington, D. C.

TABLE II

	Installations			
	I	G	U	Total
N	36	9	3	48
AG	3	9	3	15
A	9	1	14	24
Total	48	19	20	87

	Amplifiers			
	I	G	U	Total
N	3286	867	124	4277
AG	1256	544	554	2354
A	518	216	501	1235
Total	5060	1627	1179	7866

From these tables it is easily seen that the industrial nstallations have the largest average size with 105 mplifiers; the governmental installations average 86 mplifiers, and the university installations average 59 mplifiers.

The remaining data and their analysis presented in raphical form for ease of study (Fig. 1) are acumulative requency polygon showing the per cent of installations aving not more than a given number of amplifiers. For xample, 88 per cent of the installations have less than 00 amplifiers while 50 per cent of the installations have ess than 48 amplifiers. (This is a particularly interesting esult since there is an average of 90 amplifiers per in-tallation.) Further, the largest installation contains 64 amplifiers and the smallest contains 10.

Fig. 2 is a cumulative frequency polygon showing the er cent of the installations which were in service less than a given number of years as of January 1, 1955. It is immediately noted, for example, that 50 per cent of the installations were in operation less than $2\frac{1}{2}$ years while the oldest was established in 1946.

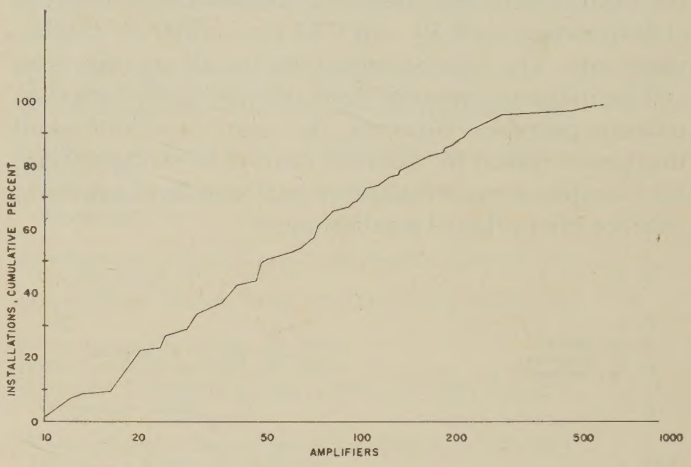

Fig. 1—Cumulative frequency polygon.

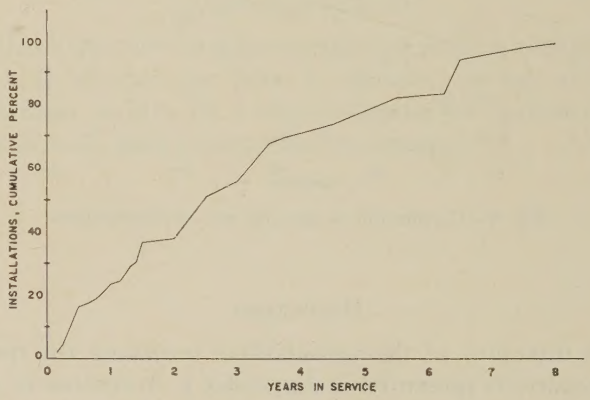

Fig. 2—Cumulative frequency polygon.

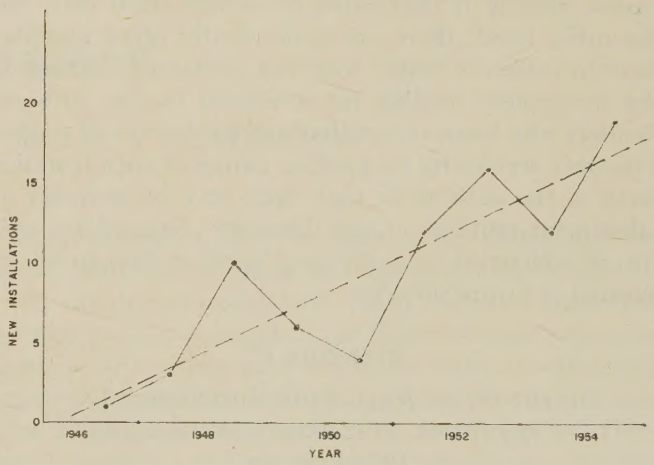

Fig. 3—New installations started each year.

Fig. 3 supplies even more growth information: the number of new installations which began each year. Although the data are extremely variable and possibly cyclic, a least-squares line has been fitted to aid in possible forecasts for the future.

Fig. 4 presents a cross-plot of the number of years in service versus the number of amplifiers. Special symbols differentiate between the various types of installations. The correlation coefficient for years in service versus the logarithm of the number of amplifiers for all types of installations is 0.59, and 0.65 for industrial installations only. The least-squares lines for all organizations and for industrial organizations alone are given for extrapolation purposes. However, the erratic variation in all the data is reason for extreme caution in extrapolating; for example, some installations may not have grown at all since their original establishment.

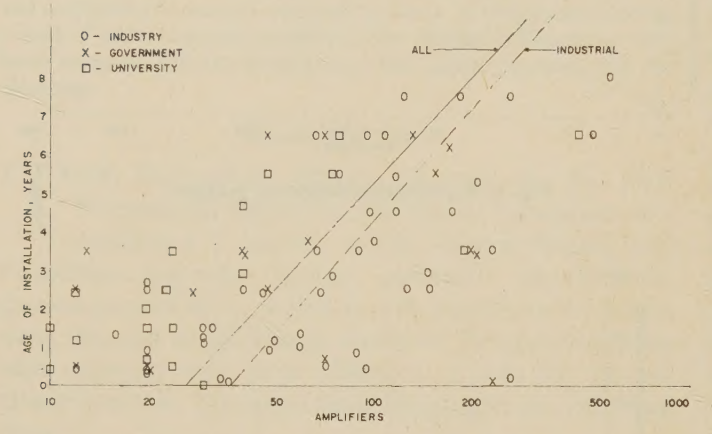

Fig. 4—Correlation of age and size of installations.

Directory

A directory of the installations returning the questionnaires is presented in Appendix I. A number of unlisted organizations are known to have electronic analog computer facilities but did not return the questionnaires, making it impossible to include them here. On the other hand, there are undoubtedly other installations in existence which were not contacted because of the incomplete mailing list available to the authors. Readers who know of installations not listed will render a distinct service by forwarding names of such installations to the authors so that they may be included in subsequent editions of the directory. Suggestions will also be welcomed for additional items of data to be requested in future surveys.

Appendix I*

Directory of Real-Time Electronic Differential Analyzer Installations
1955 Edition

Aerojet-General Corp., Azusa, Calif.	3 N
Argonne National Lab., Lamont, Ill.	3 AG
Armour Research Found., Chicago, Ill.	3 A
Battelle Memorial Inst., Columbus, Ohio	2 A
Beckman Instruments, Inc. (Berkeley Div.), Richmond, Calif.	3 A
Ballistic Research Lab. (Guidance and Control Branch, Ballistic Measurements Lab.), Aberdeen Prov. Grd., Md.	2 N
Ballistic Research Labs. (Exterior Ballistics Lab.), Aberdeen Prov. Grd., Md.	3 N
Beech Aircraft Corp., Wichita, Kan.	3 N
Bell Aircraft Corp., Buffalo, N. Y.	2 A
Bell Aircraft Corp., Buffalo, N. Y.	5 AG
Canadair Ltd., Montreal, Can.	2 N
CDC Control Services, Hatboro, Pa.	2 A
Chance Vought Aircraft, Inc., Dallas, Tex.	5 N
Collins Radio Co., Cedar Rapids, Ia.	3 N
Convair, Ft. Worth, Tex.	4 N
Convair, San Diego, Calif.	6 AG
Defense Research Lab., Austin, Tex.	2 AG
Detroit Arsenal, Center Line, Mich.	4 AG
Douglas Aircraft Co., Inc., El Segundo, Calif.	1 N
Douglas Aircraft Co., Inc., Santa Monica, Calif.	4 N
Dow Chemical Co. (Computation Lab.), Midland, Mich.	1 N
Dynalysis Dev. Labs., Inc., Los Angeles, Calif.	4 A
Electronic Associates, Inc. (Computation Center), Princeton, N. J.	4 A
Frankford Arsenal (Pitman-Dunn Lab.), Philadelphia, Pa.	3 AG
General Motors Corp. (Aeroproducts Operations, Allison Div.), Vandalia, Ohio.	3 A
Gilfillan Brothers, Inc., Los Angeles, Calif.	3 N
Glenn L. Martin Co., Baltimore, Md.	3 N
Grumman Aircraft Engrg. Corp., Bethpage, L. I.	4 N
Holloman Air Dev. Center (Computer Branch, Tech. Anal. Div., DCS/Operations), Holloman AF Base, N. Mex.	5 N
Hughes Aircraft Co. (Guided Missile Res. and Dev. Div.), Culver City, Calif.	4 N
Hughes Aircraft Co. (Radar Res. and Dev. Div.), Culver City, Calif.	5 N
Hughes Tool Co. (Aircraft Div.), Culver City, Calif.	1 N
Jack and Heintz, Inc., Cleveland, Ohio	2 N
Jet Propulsion Lab., Pasadena, Calif.	3 N
Johns Hopkins Univ. (Operations Research Office), Washington, D. C.	4 N
Leeds and Northrup Co., Philadelphia, Pa.	1 N
Lockheed Aircraft Corp., Burbank, Calif.	4 N
Louisiana State Univ. (LSU Computation Facility, Elec. Engrg. Dept.), Baton Rouge, La.	2 A
Mass. Inst. of Tech. (Dynamic Anal. and Control Lab.), Cambridge, Mass.	6 AG
W. L. Maxson Corp., New York, N. Y.	2 A
Minneapolis-Honeywell Regulator Co. (Aeronautical Div.), Minneapolis, Minn.	5 N
NACA Ames Aeronautical Lab., Moffett Field, Calif.	5 N
NACA Langley Aeronautical Lab., Langley Field, Va.	3 AG
Naval Research Lab., Washington, D. C.	3 AG
New York Univ. (College of Engrg.), New York, N. Y.	1 A
North American Aviation, Inc., Downey, Calif.	4 N
Northrop Aircraft, Inc., Hawthorne, Calif.	5 N
Northwestern Univ. (Aerial Measurements Lab.), Evanston, Ill.	3 AG
Oregon State College (Mechanical Engrg. Dept.), Corvallis, Ore.	1 A
Picatinny Arsenal (ORDBB-TRI), Dover, N. J.	1 AG
Picatinny Arsenal (ORDBB-TH1), Dover, N. J.	1 AG
Polytechnic Inst. of Brooklyn (Microwave Research Inst.), Brooklyn, N. Y.	1 A
Project Cyclone, Reeves Instrument Corp., New York, N. Y.	6 AG
Puget Sound Naval Shipyard (Planning Dept., Design Div.), Bremerton, Wash.	2 N
Purdue Univ. (Div. of Engrg. Sciences), West Lafayette, Ind.	2 N
Purdue Univ. (School of Aeronautics), West Lafayette, Ind.	2 N
Radio Corp. of America (Radar Engrg., Engrg. Products Dept., Electronic Products Div.), Moorestown, N. J.	1 N

* A: available to outsiders; AG: available to outside government contractors; N: not available to outsiders.

1: 10–20 operational amplifiers; 2: 21–40; 3: 41–80; 4: 81–160; 5: 161–320; 6: 321–640.

Ramo-Wooldridge Corp., Los Angeles, Calif. 5 N
Rand Corp., Santa Monica, Calif. 3 N
R. B. Rea Co., Inc., Santa Monica, Calif. 4 A

Redstone Arsenal (Computation Lab.), Huntsville, Ala. 2 N
Rensselaer Polytechnic Inst. (Computer Lab.), Troy, N. Y. 2 A
Republic Aviation Corp. (Guided Missiles Div.), Hicksville, L. I. 2 N
Sandia Corp., Sandia Base, Albuquerque, N. Mex. 3 N
Schlumberger Well Surveying Corp. (Research Labs.), Ridgefield, Conn. 2 N

Southern Research Inst., Birmingham, Ala. 1 A
Sperry Corp. (Sperry Gyroscope Co. Div.), Great Neck, N. Y. 4 N
Sperry Corp. (Sperry Gyroscope Co. Div.), Great Neck, N. Y. 4 N
Sperry Corp. (Sperry Gyroscope Co. Div.), Great Neck, N. Y. 3 N
Sperry Corp. (Sperry Gyroscope Co. Div.), Great Neck, N. Y. 3 N

Taylor Model Basin (Code 535), Navy Dept., Washington, D. C. 2 N
Technical Operations, Inc., Arlington, Mass. 2 A
Temco Aircraft Corp., Dallas, Tex. 2 N
Univ. of Buffalo (Physics Dept.), Buffalo, N. Y. 1 A
Univ. of California (Electrical Engrg. Div.), Berkeley, Calif. 1 A

Univ. of Colorado (Engrg. Experiment Station), Boulder, Colo. 1 A
Univ. of Kansas (Dept. of Elec. Engrg.), Lawrence, Kan. 1 A
Univ. of Michigan (Willow Run Res. Center, Engrg. Res. Inst.), Ypsilanti, Mich. 5 A
Univ. of Minnesota (College of Engrg., Inst. of Technology), Minneapolis, Minn. 2 A
USNAMTC (Simulation Lab.), Pt. Mugu, Calif. 4 AG

U. S. Naval Gun Factory (Physics Branch, Code 724), Washington, D. C. 1 AG
U. S. Naval Ordnance Lab., Corona, Calif. 3 N
U. S. Naval Ordnance Lab., Corona, Calif. 5 A
U. S. Naval Postgraduate School (Dept. of Math. and Mechanics), Monterey, Calif. 1 AG
U. S. Naval Postgraduate School (Elec. Engrg. Dept.), Monterey, Calif. 1 N

U. S. Navy Electronics Lab., San Diego, Calif. 1 AG
U. S. Navy Electronics Lab., San Diego, Calif. 1 N
Westinghouse Electric Corp. (Control Engrg. Dept), Buffalo, N. Y. 1 N
Westinghouse Electric Corp. (Aviation Engrg. Dept.), Lima, Ohio 1 N
Westinghouse Electric Corp. (Atomic Power Div.), Pittsburgh, Pa. 3 N

Westinghouse Electric Corp. (Analytical Section 5-L-51), E. Pittsburgh, Pa. 4 N
Westinghouse Electric Corp. (Air Arm Div.), Baltimore, Md. 4 N
White Sands Prov. Grd., N. Mex. 3 N
White Sands Prov. Grd., N. Mex. 5 N
Worcester Polytechnic Inst. (Dept. of Elec. Engrg.), Worcester, Mass. 1 A

Wright Air Dev. Center (Aeronautical Res. Lab.), Wright-Patterson AF Base, Ohio. 4 AG

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A Digital Computer for Use in an Operational Flight Trainer*

W. H. DUNN, C. ELDERT, AND P. V. LEVONIAN†

Summary—**The requirements for a digital computer for use in an operational flight trainer are presented with emphasis being placed on the real-time aspects of the problem. The general purpose digital computer is shown to be inadequate for this purpose and a special purpose digital computer is described which meets the requirements.**

INTRODUCTION

A REAL-TIME simulator is a device which simulates a physical system, responding to external stimuli as fast as does the actual system. In the case of the operational flight trainer, the simulator is required to sense pilot's actions and actuate cockpit instruments so fast that the pilot cannot distinguish between simulator response and true airplane response.

In the digital operational flight trainer a numerical or step-by-step solution of the flight systems' equations is made with a time interval chosen which is sufficiently small to ensure accuracy and stability of the solution. The flight system as simulated by the trainer described here involves a system of ten simultaneous nonlinear differential equations with the forces and moments being under the indirect control of the pilot. In order for the digital flight trainer to simulate the flight system in real-time, it is required once each time interval to (a) sample the pilot's commands (through examination of the throttle, control surface deflections, etc.), (b) make a numerical solution of the systems equations, and (c)

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render a reading to all of the cockpit instruments. The total time for performing these three operations must, of course, be equal to or less than the chosen time interval.

Through studies made at the Moore School,[1] the time interval permitted for a stable and accurate numerical solution of the systems equations with the integrating formulas used was found to be 50 milliseconds.

Programming for the solution of the flight equations with a one-address code showed that the total number of digital computer operations required was 1,150. This included approximately 450 additions and subtractions, 250 multiplications, 15 divisions, 25 transfer of control operations, 120 shifts and 290 transfers from arithmetic unit to memory.

Investigation of the fastest general purpose digital computers in existence showed that the minimum time in which the above operations could be performed was 100 milliseconds. It was therefore concluded that the real-time solution of the systems equations was not possible with existing general purpose digital computers.

To the time required for the solution of the flight equations must be added the time needed for the reading-in of the pilot's sampled control commands and the reading-out of the computed results to the several cockpit instruments. The time consumed by conventional input-output equipment used by general purpose computers is, of course, prohibitive for the simulator application. Furthermore, the data as presented by this equipment are not in a form which can be used by the simulator. To keep the read-in and read-out times of the simulator at a minimum the requirement is imposed that these operations take place at the same speed or nearly the same speed as the normal transfer of data within the computer itself.

The input to the simulator therefore requires the use of an analog-to-digital converter which is able to sample the analog control commands of the pilot (position of the throttle, stick, etc.) and to convert them to a digital form which can be read into the computer at a rate very nearly equal to the computer's synchronous speed.

The computed results of the flight equations are not generally in a form readily understood by the pilot. Hence, additional arithmetic manipulation of these results is necessary to put them in the correct form. It has been found that approximately 700 separate computer operations are required for this purpose. The output process requires first that the computed results be transformed to the correct digital forms; and then that these digital values be read from the computer, at the computer's synchronous speed, to a digital-to-analog converter where they can be converted to analog forms capable of operating the cockpit instruments.

It can be seen that the conversion equipment described above must operate at great speeds in order to keep pace with the computer.

[1] H. J. Gray, Jr., "Numerical methods in digital real-time simulation," *Quart. Appl. Math.*, vol. 12, pp. 133–140; July, 1954.

The precision of the simulator need not be as large as that used by the general purpose computer. Mathematical investigation of the effect of truncation and round-off errors on the solution of the flight equations indicated that the use of 20 binary digits was adequate. This reduction in precision permits an increase in the speed of the simulator.

The first portion of this paper has discussed the reasons for the inadequacy of the general purpose digital computer for the flight trainer application. The primary reason was shown to be the speed requirement. The remainder of the paper will be devoted to a logical description of a special purpose digital computer which is capable of the real-time solution of the problem described. The basic philosophy of the computer is first discussed and a list of the orders performed by it is given. Next the block diagram of the computer is presented. Finally, the logical details of two arithmetic units which conform to the basic philosophy and to the block diagram are described. The description of the input-output equipment is omitted. The details of this equipment are to be found elsewhere.[2]

Basic Philosophy

During the study of a digital computer for real-time simulation four basic features emerged to make possible a machine of the required speed.[3] The first three of these are applicable to any pulse-type computer while the fourth finds use only if a serial memory is employed. Although efficient use of a machine embodying these principles requires some effort on the part of the programmer, this is considered justified because the computer application is special purpose. The four features, not necessarily in order of importance are (a) the partitioning of the memory into separate and distinct number and instruction memories, (b) the use of a one-address code, a multiply-add register (MAR) and a transfer-clear-add instruction (TCA), (c) the incorporation of a high speed multiplier, and (d) the use of a small, short tank memory unit (NSF) in addition to the main number memory.

Partitioning of the Memory

Separate and distinct number and instruction memories make possible the decoding of orders while arithmetic operations are in progress. Since different output busses exist for the two memories, the succeeding instruction may be decoded just before the completion of the current arithmetic operation. Therefore, the decoding of orders consumes no routine time.

It should be noted that with this memory arrangement modification of orders is not possible. The loss of this feature is not important, however, due to the special nature of the computer.

[2] "Universal Digital Operational Flight Trainers," University of Pennsylvania, Moore School Res. Div., Rept. 54-45; June 30, 1954.

[3] Portions of the basic philosophy were suggested by H. J. Gray, Jr., "The organization of a digital real-time simulator," 1953 IRE Convention Record, Part 1, "Radar and Telemetry," pp. 85–88.

One-Address Code, MAR and TCA

The purpose of these features is to minimize the unnecessary transferring of numbers between the arithmetic unit and the number memory. Since a one-address code is used, the arithmetic unit contains an accumulator which may store result of an arithmetic operation without requiring its return to the number memory.

In the solution of the flight equations, there are numerous occasions when the sum of products must be formed. To facilitate this type of operation the arithmetic unit contains, in addition to the main accumulator, an accumulating register (MAR). In the normal one-address operation each product must be individually formed and returned to the number memory and then the summation made. With the additional accumulating register each product may be accumulated in the MAR as it is formed by the multiplier unit in the main accumulator and no transfers to the number memory are necessary. In effect, the evaluation of the succeeding product may begin while the accumulation of the current product is taking place in MAR.

Since the numerical solution of differential equations involves the replacement of "past history" ordinates and derivatives as the computation proceeds, it is convenient to incorporate the TCA instruction in the machine. This order permits the simultaneous transfer of the contents of the main accumulator to the specified number memory register, and the addition of the previous number in the register into the cleared accumulator. Therefore, the time required to transfer "past history" is approximately half that necessary without TCA.

High Speed Multiplier

Since multiplication generally consumes a considerable portion of routine time, a high speed multiplier is used. This permits successive multiplications to proceed at the rate of one every two addition times.

NSF

In order to attain a high percentage of minimum time programming with a serial memory, an auxiliary number memory unit, NSF, is incorporated. NSF consists of three short tanks of individual length such that minor cycle positions in each short tank precess in time with respect to corresponding minor cycle positions both in the main number memory and in the other two NSF tanks. During certain operations (add, multiply, transfer, etc.) it is possible to transfer the operand specified by the instruction into one of the NSF tanks concurrently with the performance of the principal instruction; numbers may be called from NSF since each tank is assigned a number memory address. Therefore, it is possible to perform an operation with an operand in any number memory location, transfer it into NSF with no loss of time, and use it later in the routine when it would not otherwise be available in the first number memory location. This technique greatly enhances minimum time programming without the expense of an equivalent amount of one-word storage.

List of Instructions

As a consequence of the basic philosophy given above, numerical operations are performed in the arithmetic unit according to the instructions listed below. For a computer with serial memory the first seven orders listed are performed in conjunction with NSF. Additional order types (not included below) control such operations as input-output.

In the following listing, a is the number stored in the main accumulator and b is the contents of the number memory address specified with the order type.

1. *Add.* Form the sum a plus b and store it in the main accumulator.
2. *Subtract.* Form the difference a minus b and store it in the main accumulator.
3. *Multiply.* Form the product a times b and store it in the main accumulator.
4. *Multiply-Add.* Form the product a times b and accumulate it in the multiply-add register. Clear the main accumulator.
5. *Square.* Form the product b times b and store it in the main accumulator.
6. *Transfer.* Transfer a to the specified number memory address, erasing b.
7. *Transfer-Clear.* Transfer a to the specified number memory address, erasing b. Clear the main accumulator.
8. *Absolute-Add.* Form the sum a plus the absolute value of b and store it in the main accumulator.
9. *Absolute-Subtract.* Form the difference a minus the absolute value of b and store it in the main accumulator.
10. *Divide.* Form the quotient a divided by b and store it in the main accumulator.
11. *Shift.* Shift a to the left or right n places as specified by the "number memory" address.
12. *Shift-Add.* Shift a to the left or right n places as specified by the "number memory" address. Accumulate the shifted number in the multiply-add register and clear the main accumulator.
13. *Transfer-Clear-Add.* Transfer a to the specified number memory address and clear the main accumulator. Add b into the main accumulator. (This order is performed in one addition time.)
14. *Compare.* Alter the sequence of instructions if the algebraic sign of a is negative.

Block Diagram of the Computer

The basic philosophy enumerated above is shown for a serial memory computer by block diagram of Fig. 1 (next page). The order memory tanks are sequenced by means of the order memory sequencing counter normally advanced after all the orders in a tank have been performed. The coded output of the counter is

decoded by the order memory address decoder which selects that tank in the order memory corresponding to the state of the counter. Note that the selection of an order requires the specification of only the tank within which the order lies and not its particular position (minor cycle) within the tank; minor cycle specification is unnecessary since all orders within a tank are programmed in sequence.

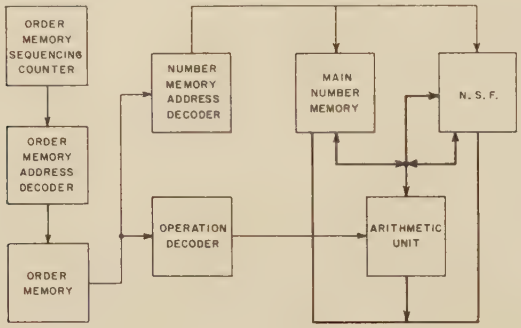


Fig. 1—Block diagram of computer.

The one-address output of the order memory is sent to two units: the instruction goes to the operation decoder which controls operation of the arithmetic unit; the address goes to the number memory address decoder which selects that tank in the number memory corresponding to the coded address. Again, only the tank within which the number lies is specified; this implies that all numbers must be stored such that they are available for computation in the arithmetic unit exactly when needed.

The dark lines in Fig. 1 indicate number flow among the main number memory, NSF and arithmetic unit.

The separation of the memories makes possible simultaneous access to orders and numbers. The manner in which orders and numbers are withdrawn from the memories to perform a sequence of instructions is illustrated in Fig. 2. During minor cycle 1 the instruction "add a" is decoded and the arithmetic unit is cleared.

MINOR CYCLE	1	2	3	4	5
ORDER BEING DECODED IN CONTROL	ADD a	ADD b	ADD c	ADD d	—
ORDER BEING PERFORMED IN ARITH. UNIT	CLEAR	0 + a	a + b	(a+b)+c	(a+b+c)+d
RESULT LEFT IN ARITH. UNIT AT END OF MINOR CYCLE	0	a	a + b	a+b+c	a+b+c+d

Fig. 2—Evaluation of $a+b+c+d$.

During minor cycle 2, a is added into the arithmetic unit and simultaneously the instruction "add b" is decoded; at the end of minor cycle 2 the arithmetic unit contains a. Remainder of process may be followed from Fig. 2.

The multiply-add register and the fast multiplier will be discussed in the detailed description of the arithmetic unit, which follows.

Arithmetic Unit

Two arithmetic units are described: the first is serial throughout while the second incorporates features of both serial and parallel operation. Both are ac coupled and use conventional OR-AND-OR logical pyramids. Number representation is absolute magnitude (less than 1) and algebraic sign. The arithmetic units described here handle numbers of twenty bit magnitude although other precisions may be employed. While a serial memory is assumed in the following discussion, a fast random access memory can be used as an alternative.

Serial Arithmetic Unit[4]

A simplified logical diagram of the serial arithmetic unit is shown in Fig. 3. The control outputs of the operations decoder are indicated by numerals enclosed by hexagons; when referred to in the text, these numerals are shown in parentheses. A description of the operation for the various instructions follows.

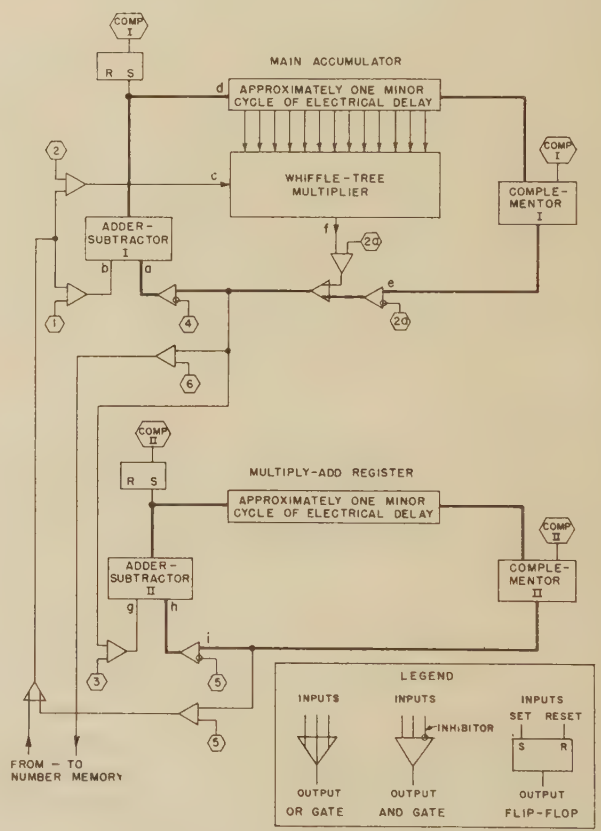


Fig. 3—Basic logic of serial arithmetic unit.

Add and Subtract. In the add and subtract operations the number from the memory is gated by (*1*) to the b input of adder-subtractor I. Simultaneously, the number within the accumulator (the result of the previous operation) enters the a input. Both numbers enter the adder-subtractor least significant digit first. The number

[4] For greater details, see P. V. Levonian, "The Functional Description of a Digital Real Time Simulator," Master's Thesis at the Moore School of Electrical Engineering, University of Pennsylvania; June, 1953.

MINOR CYCLE	1	2	3	4	5	6	7	8
ORDER DECODED IN CONTROL.	ADD a	MULTIPLY b	ADD c	MULTIPLY d	BLANK	MULTIPLY e	ADD f	——
OPERATION PERFORMED IN ARITHMETIC UNIT	ACCUMULATOR CLEARED	a ADDED TO ZERO	a MULTIPLIED BY b: L.S. DIGITS FORMED AND DISCARDED	a MULTIPLIED BY b: M.S. DIGITS FORMED; c ADDED TO M.S DIGITS	(ab+c) MULTIPLIED BY d: L.S. DIGITS FORMED AND DISCARDED	(ab+c) MULTIPLIED BY d: M.S. DIGITS FORMED	(ab+c)d MULTIPLIED BY e: L S DIGITS FORMED AND DISCARDED	(ab+c)d MULTIPLIED BY e: M.S DIGITS FORMED; f ADDED TO M.S.DIGITS
CONTENTS OF A.U. AT END OF MINOR CYCLE.	0	a	——	ab+c	——	(ab+c)d	——	(ab+c)de+f

Fig. 4—Evaluation of $(ab+c)de+f$.

at b is serially added to or subtracted from the number at a depending on the instruction and the algebraic signs of the two operands. The result circulates through one minor cycle of delay in the main accumulator loop (shown in heavy lines) and returns to the a input of adder-subtractor I in time to be operated upon by the next instruction. Successive additions or subtractions take place in successive minor cycles.

If a subtraction is performed in which the magnitude of the subtrahend exceeds that of the minuend, the output of adder-subtractor I is the two's complement of the difference. Borrow digits are formed to the left of the most significant place and the first of these is detected by the flip-flop which generates the output (COMP I). (COMP I) energizes complementor I which re-complements the result, restoring it to absolute magnitude form in time to enter the a input of the adder-subtractor for the next operation.

Multiply. Multiplication is performed by the whiffle-tree multiplier of Fig. 3 (previous page) which develops a full product in two minor cycles. During the first minor cycle the number from the memory (multiplier) is gated into the whiffle-tree by (*2*); there it operates on the number circulating in the main accumulator loop (multiplicand) to form the low order product which appears at f and is discarded. During the second minor cycle the whiffle-tree continues to operate on the multiplicand and the high order product is developed. Control (*2a*) blocks recirculation of the multiplicand at e and gates the high order product into the main accumulator loop in its stead.

A further operation may take place in the adder-subtractor during the second minor cycle because the high order product appears at f, least significant digit first, in synchronism with the normal recirculation timing at e. Therefore, multiplication effectively takes one minor cycle to perform, with a single exception. Two multiplications can not be performed in successive minor cycles since the whiffle-tree is occupied for two minor cycles per multiplication. In this case a blank order must be programmed between the two multiply orders. The above processes are illustrated in Fig. 4 for the evaluation of the expression $(ab+c)\,de+f$.

A whiffle-tree multiplier for four-digit numbers is illustrated in Fig. 5. The multiplier enters serially, least significant digit first, at point c. Each digit is gated by a timing pulse (the least significant by *T1* and the most significant by *T4*) to set one of the flip-flops if the digit is a "one." Each set flip-flop is reset one minor cycle later. Simultaneously with the entrance of the multiplier, the multiplicand enters, least significant digit first, at point d. The latter appears immediately at "and gate" 1, is delayed one pulse time before arriving at "and gate" 2, etc.; each pulse time of delay shifts the multiplicand one place to the left. Each digit of the multiplier (stored in the flip-flops) gates the properly shifted multiplicand into the adders whose final output is the product. This process may be easily expanded for any number of digits. An example of the operation of the whiffle-tree multiplier is shown in Fig. 6.

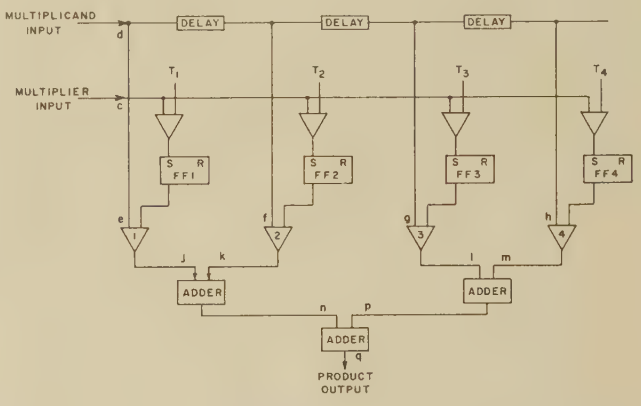


Fig. 5—Four-digit whiffle-tree multiplier.

MINOR CYCLE 2				MINOR CYCLE 1				TIME ← / LOCATION
T_4	T_3	T_2	T_1	T_4	T_3	T_2	T_1	
0	0	0	0	1	1	1	1	FF-1
0	0	0	1	1	1	1	0	FF-2
0	0	0	0	0	0	0	0	FF-3
0	1	1	1	1	0	0	0	FF-4
0	0	0	0	1	1	0	1	e
0	0	0	1	1	0	1	0	f
0	0	1	1	0	1	0	0	g
0	1	1	0	1	0	0	0	h
0	0	0	0	1	1	0	1	j
0	0	0	1	1	0	1	0	k
0	0	0	0	0	0	0	0	l
0	1	1	0	1	0	0	0	m
0	0	1	0	0	1	1	1	n=j+k
0	1	1	0	1	0	0	0	p=l+m
1	0	0	0	1	1	1	1	q=h+p

MOST SIGNIFICANT HALF OF PRODUCT — LEAST SIGNIFICANT HALF OF PRODUCT

MULTIPLIER −1011
MULTIPLICAND −1101

Fig. 6—Example of four-digit multiplication in whiffle-tree multiplier.

The flip-flops, gates and adders of Fig. 5 are included in the block marked "Whiffle-Tree Multiplier" in Fig. 3.

MINOR CYCLE	1	2	3	4	5	6	7	8
ORDER DECODED IN CONTROL.	ADD a	MULTIPLY ADD b	ADD c	MULTIPLY ADD d	ADD e	MULTIPLY f	ADD M.A. REG.	——
OPERATION PERFORMED IN ACCUMULATOR	ACCUMULATOR CLEARED	a ADDED TO ZERO	a MULTIPLIED BY b: L.S. DIGITS FORMED AND DISCARDED	a MULTIPLIED BY b: M.S. DIGITS FORMED; c ADDED TO ZERO	c MULTIPLIED BY d: L.S. DIGITS FORMED AND DISCARDED	c MULTIPLIED BY d: M.S. DIGITS FORMED; e ADDED TO ZERO	e MULTIPLIED BY f: L.S. DIGITS FORMED AND DISCARDED	e MULTIPLIED BY f: M.S. DIGITS FORMED; ab+cd ADDED TO M.S. DIGITS
OPERATION PERFORMED IN M.A. REGISTER	——	——	——	ab ADDED TO ZERO	——	cd ADDED TO ab	——	ab+cd READ OUT REG. CLEARED
CONTENTS OF ACC. AT END OF MINOR CYCLE	0	a	——	c	——	e	——	ab+cd+ef
CONTENTS OF M.A. REGISTER AT END OF MINOR CYCLE	0	0	0	ab	ab	ab+cd	ab+cd	0

Fig. 7—Evaluation of $ab+cd+ef$

The shifting of the multiplicand is performed by the electrical delay of the main accumulator loop. Since the flip-flops of the whiffle-tree are reset one minor cycle after they are set, the result of an operation during the second minor cycle can circulate in the main accumulator without disturbing the whiffle-tree.

Multiply-Add. In the multiply-add instruction multiplication is performed as previously described. The most significant half of the product is prevented from circulating in the main accumulator by (*4*) and, instead, is gated by (*3*) to the *g* input of adder-subtractor II. There it is added to or subtracted from the previous contents of the multiply-add register. The operation of complementor II in the multiply-add register is identical with that of complementor I in the main accumulator. Simultaneously with the accumulation of the product in the multiply-add register, a number from the memory may be read into the cleared accumulator.

When the address of the multiply-add register is specified, control (*5*) gates its contents to the memory output bus. Simultaneously, (*5*) blocks recirculation in the register, clearing it for the next summation of products. The use of the multiply-add order in evaluating the sum of products is illustrated in Fig. 7 for the expression $ab+cd+ef$.

Divide. The divide operation is performed by a conventional nonrestoring process. The number in the arithmetic unit (the result of the previous operation) is the dividend, while the number from the memory is the divisor. The divisor is stored in a one number storage register (not shown in Fig. 3). The additions or subtractions and storage of partial remainders take place in the multiply-add register, while the quotient digits are stored in the main accumularor as they are formed. To obtain the twenty-digit quotient, twenty minor cycles are required. This time is not prohibitively long since relatively few divisions are encountered. Furthermore, transfers from the main number memory to the NSF unit may be made while the divide operation is in progress.

Shift. The number stored in the main accumulator is shifted to the left or right by effectively lengthening or shortening the normal one minor cycle delay of the accumulator loop. Shifts up to fourteen places in either direction are possible in one minor cycle.

Shift-Add. In the shift-add operation the number stored in the main accumulator is shifted as described above. It is then accumulated in the multiply-add register (as described previously) and the main accumulator is cleared. The order is useful in the evaluation of such expressions as $2^{-3}a+2^{7}b-2^{5}c$.

Transfer. In the transfer instruction the number in the main accumulator is permitted to recirculate, but is gated by (*6*) onto the memory input bus and stored in the specified address. The operation time required is one minor cycle.

Transfer-Clear. In this order the number in the main accumulator is transferred to the memory as described above. The accumulator is cleared by control (*4*).

Speed. The speed of the serial arithmetic unit assuming a 1 megacycle pulse repetition rate and a twenty bit precision is given in Fig. 8.

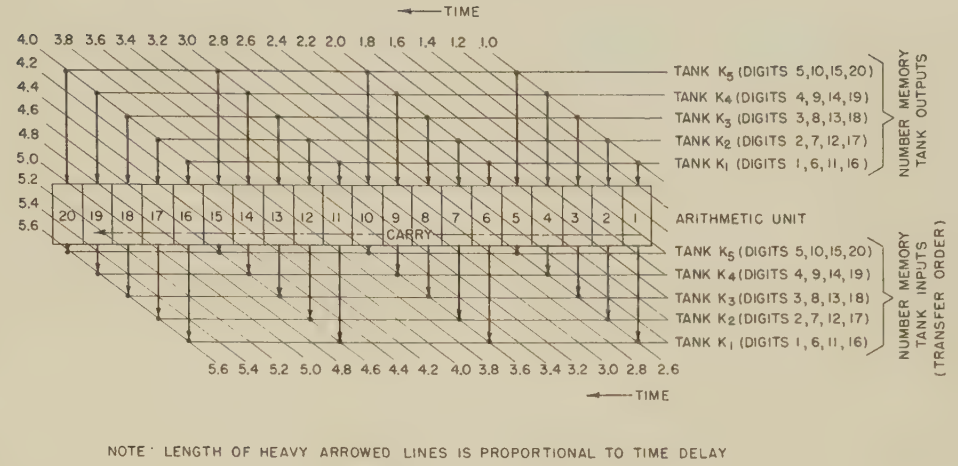
OPERATION	TIME (MICROSECONDS)
ADD	24
SUBTRACT	24
ABSOLUTE – ADD	24
ABSOLUTE – SUBTRACT	24
TRANSFER	24
TRANSFER–CLEAR–ADD	24
SHIFT (2^{14} OR 2^{-14} MAX)	24
COMPARE	24
MULTIPLY, MULTIPLY–ADD, SQUARE	24 EXCEPT WHEN FOLLOWED BY AN (M), (MA) OR (SQ) ORDER IN WHICH CASE 48 ARE REQUIRED
DIVIDE	480

Fig. 8—Operation times for serial arithmetic unit at 1 mc repetition rate, twenty bit magnitude numbers.

Sequential Arithmetic Unit[5]

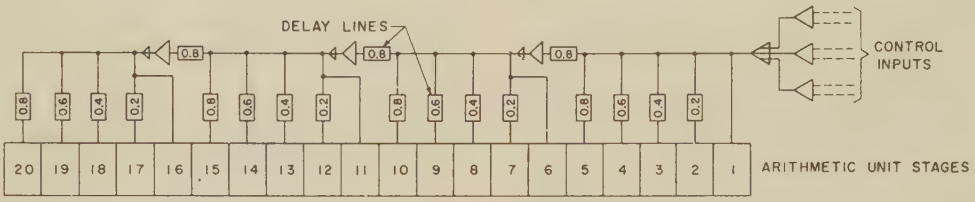
As a further means of decreasing computation time it is convenient to replace the serial arithmetic unit previously described by one whose operation is fashioned after that of both a parallel and a serial machine. The result is termed a "sequential" arithmetic unit which combines the stage duplication of a dc coupled computer with the controlled carry time of a pulse-type machine. Thus, the arithmetic unit consists of a connected series of identical stages, each stage performing the same operations on a single number column. Furthermore, like operations in adjacent stages are always delayed the time required to generate a possible carry. Conse-

[5] For greater detail, see "Design Description of the UDOFT," University of Pennsylvania, Moore School Research Division, Rept. 55-05; September 6, 1954.



NOTE: LENGTH OF HEAVY ARROWED LINES IS PROPORTIONAL TO TIME DELAY

Fig. 9—Sequential arithmetic unit timing.



NOTES: 1. NOMINAL LENGTHS OF DELAY LINES INDICATED IN FRACTIONS OF A PULSE TIME.
2. OUTPUTS OF DISPATCHER LINE CONNECT TO LIKE POINTS IN EACH STAGE OF THE ARITHMETIC UNIT.

Fig. 10—Typical dispatcher line.

quently, arithmetic operation times are independent of whether or not ripple carries are generated.

Arithmetic Unit and Number Memory—General Timing Considerations. Because the logical structure of the arithmetic unit and the manner of storing numbers in the memory are influenced by the number of clock phases per pulse time, a factor is chosen that may be met in practice. In the following discussion five clock phases per pulse time are assumed; i.e., the nominal delay through an OR-AND-OR pyramid is 0.2 pulse times.

In the number memory each address refers to five acoustic tanks which store pulses serially at one pulse time intervals. *Tank* K_1 (see Fig. 9) contains pulse positions 1, 6, 11 and 16 of each number while *tank* K_5 stores pulse positions 5, 10, 15 and 20; pulse position 1 is synchronous with pulse position 5, and 16 with 20.

When reading from the number memory to the arithmetic unit, bits 1 through 5 are simultaneously gated from the memory at time 1.0, and are delayed to arrive at the arithmetic unit displaced one clock phase between digits, least significant digit first; digits 16 through 20 arrive at the arithmetic unit at times 4.2 through 5.0 respectively. In order to gate the proper digit into each stage of the arithmetic unit, a dispatcher line (Fig. 10) is used. A single control pulse introduced into this line at time 1.0 gates pulse position 1 into stage 1 at time 1.2, and gates pulse position 20 into stage 20 at time 5.0.

Since one clock-phase delay is spent in generating a possible carry in each stage, the carry propagates through the arithmetic unit in synchronism with the arrival of digits from the memory.

When transferring from the arithmetic unit to the number memory, pulse position 1 is delayed 0.8 pulse times to arrive at *tank* K_1 at the same time, 2.6, that digit 5 arrives at *tank* K_5; the outputs of stages 16 through 20 are accepted at *tanks* K_1 through K_5 at time 5.6. An electrical delay line is inserted in the recirculation path between the read-out and read-in gates of each tank in order to transfer numbers "on time."

From the above, the total time required to read a number into or out of the arithmetic unit is twenty clock phases for twenty bit magnitude numbers. This is equivalent to four pulse times when five clock phases per pulse time are used. Two additional pulse times are allowed for the initiation of recomplementation in subtraction or for truncation in the event of an exceed capacity in addition; because it is not necessary to wait for the second possible carry to propagate fully before reading the next number from the memory, a six pulse-time minor cycle suffices. The remainder of each minor cycle in the number memory is used to store an algebraic sign and five parity digits. The decision to use an absolute magnitude and algebraic sign number representation is dictated in part by the unavailability of a mem-

ory that (a) could "keep time" with the possible speed of the arithmetic unit using complement forms, and that (b) would still permit efficient programming.

Logic of the Arithmetic Unit. A simplified logical diagram of the four least significant stages of the arithmetic unit is shown in Fig. 11. The basic structure per stage (which is repeated twenty times for twenty precision place numbers) consists of a three-input binary adder, a three-input binary adder-subtractor, a dynamic flip-flop, three gating amplifiers and a recirculation delay line. In the figure, numerals enclosed by hexagons refer to the outputs of eight dispatcher lines while M and T signify multiplication and transfer controls respectively; the symbols U, UC and LC refer to the units, upper carry and lower carry outputs of each stage.

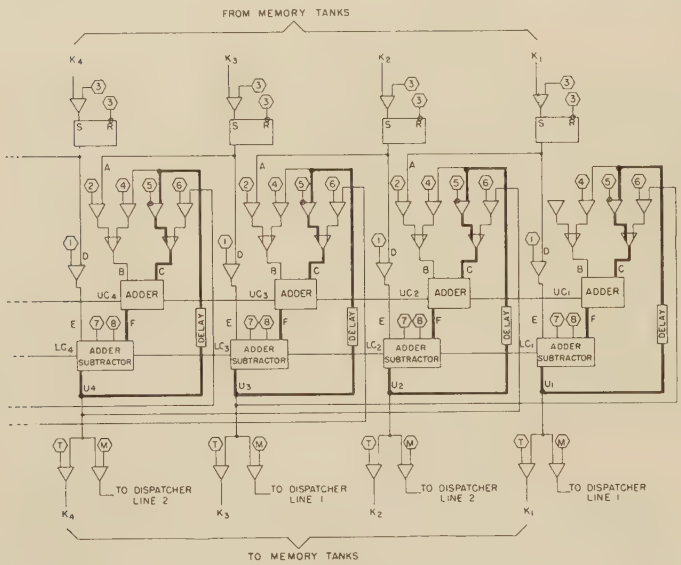


Fig. 11—Basic logic of four least significant stages of sequential arithmetic unit.

Storage. The result of the previous operation is normally stored in the accumulator loops depicted by the heavy lines. The total delay around each loop is one pulse time, each loop storing one digit of the number.

Clearing. The accumulator loops are cleared by pulsing dispatcher line (*5*) once.

Addition. The number from the memory is gated into the adder-subtractors by pulsing (*3*) and (*1*) once (when the flip-flops are set and reset simultaneously, set predominates). There it is added to the digits circulating in the accumulator loops and the new sum stored. A carry from the twentieth adder-subtractor LC_{20} is used to detect exceed capacity.

Subtraction. The number from the memory is gated into the adder-subtractors as in the addition operation. There it is subtracted from the digits circulating in the accumulator loops by pulsing (*8*) once. If the magnitude of the subtrahend is greater than that of the minuend, the result appears in two's complement form which is detected by a carry from the twentieth adder-subtractor. Re-complementation is performed by pulsing (*7*) once, and reversing state of algebraic sign counter.

Shift Left. The number in the accumulator loops is shifted left n places by pulsing (*4*) n times. Each pulse causes the contents of each loop to be added to itself; i.e. shift left is mechanized by doubling.

Shift Right. The number in the accumulator loops is shifted right $2n$ places by pulsing (*5*) and (*6*) n times. Each pair of pulses blocks the normal circulation paths and gates the digit of each loop into the loop two stages to its right. A shift right of $2n-1$ places is effected by shifting left one place before shifting right.

Multiplication. Multiplication is performed by a two-tier multiplier consisting of the upper row of adders and the lower row of adder-subtractors (functioning as adders) which together permit the addition of three numbers simultaneously. The multiplicand is read from the memory and stored in the dynamic flip-flops by pulsing (*3*) once. The number in the accumulator loops (multiplier) is separated into odd- and even-column digits which are serialized and sent down dispatcher lines (*1*) and (*2*) respectively, least significant digit first. The accumulator loops are cleared by pulsing (*5*). Dispatcher lines (*1*) and (*2*) gate the multiplicand into the adder-subtractors and adders unshifted and shifted left one place according to the two least significant digits of the multiplier. The resultant partial product is shifted right two places by pulsing (*5*) and (*6*), and is added to the multiplicand as gated by the next two digits of the multiplier appearing on (*1*) and (*2*). After this sequence has been repeated ten times, the twenty most significant digits of the product have been formed and the twenty least significant digits have been discarded.

In multiplication, the algebraic sign of the product is determined immediately and the product itself is always in absolute magnitude form. Therefore, one pulse time after the least significant digit of the high order product has been formed, the next order may commence in the least significant stage; it is not necessary to wait for the final carry to propagate fully before starting the next operation.

In illustration, the multiplication of two 4-digit numbers is shown in Fig. 12. Letters not previously defined refer to locations in Fig. 11.

Consider for example stages 1 and 2. At time 1.4, C of stage 1 is cleared by control pulse (*5*) while the two least significant multiplier digits gate the least significant multiplicand digit at D and A. Consequently, at time 1.6 the least significant multiplicand digit (a "one") arrives at E and nothing at F in stage 1; there is no A input for stage 1. Still at time 1.6, (i) the least significant multiplier digit gates the second least significant multiplicand digit at D in stage 2, (ii) the multiplicand digit from stage 1 appears at B in stage 2 as a result of the previous gating at time 1.4 by (*2*), (iii) C in stage 2 is zero as a result of clearing by (*5*), and (iv) there is no carry UC_1.

At time 1.8, the units digit U_1 (a "one") is emitted by the adder-subtractor of stage 1, ready to be shifted two places to the right (and hence off the accumulator),

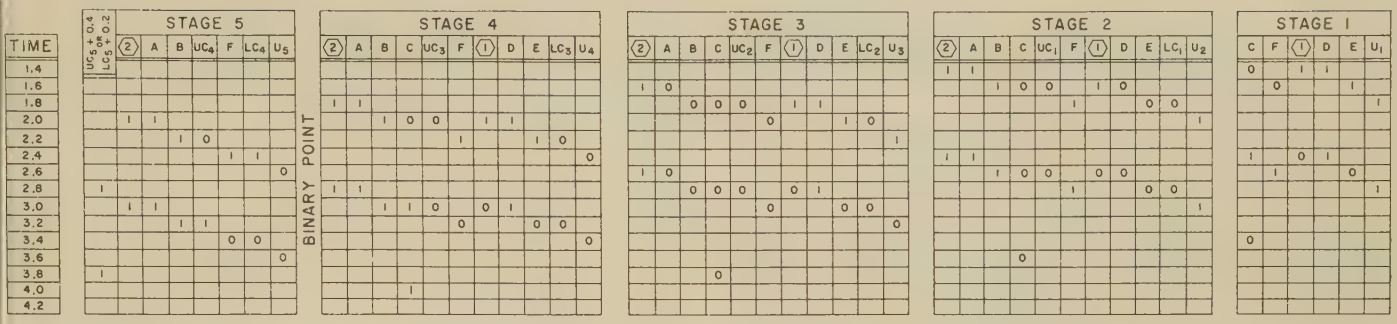


Fig. 12—Multiplication timing chart.

and the carry LC_1 (a "zero") is generated. At the same time in stage 2, (i) the output of the adder arrives at F, (ii) the multiplicand digit (a "zero") arrives at E, and (iii) the carry from the adder-subtractor of stage 1 arrives at the adder-subtractor of stage 2.

At time 2.0, stage 1 has completed all its preceding gating, while the adder-subtractor of stage 2 emits as its units output a "one" (the sum of E, F and LC_1), and as its carry output a "zero."

The remainder of the process may be followed from Fig. 12 in similar fashion.

Division. A nonrestoring division process is used in which the number stored in the accumulator loops as the result of the previous operation is divided by the number specified in the divide order. During division, the divisor is stored in the dynamic flip-flops and the necessary additions, subtractions and shifts are performed in the accumulator loops as described above. The quotient digits are stored in an additional register as they are formed, and the complete quotient is returned to the accumulator loops at the end of the division.

Multiply-Add. In order to perform the multiply-add instruction an additional accumulating register is included. As the high order digits of the product are formed, they are sent to this register and the main accumulator is cleared.

OPERATION	TIME (MICROSECONDS)
ADD	5
SUBTRACT	5
ABSOLUTE - ADD	5
ABSOLUTE - SUBTRACT	5
TRANSFER	5
TRANSFER - CLEAR	5
TRANSFER - CLEAR - ADD	5
SHIFT (2^5 OR 2^{-8} MAX)	5
COMPARE	5
MULTIPLY	10
MULTIPLY - ADD	10
SQUARE	10
DIVIDE	105

Fig. 13—Operation times for sequential arithmetic unit at 1.2 mc repetition rate, twenty bit magnitude numbers.

Speed. The speed of the sequential arithmetic unit for the various operations is given in Fig. 13. These speeds assume a 1.2 megacycle pulse repetition rate and a precision of twenty bits.

Conclusions

The problem outlined in the introduction was programmed for the computer described in this paper. Using a serial acoustic memory, with as many as 100 words stored per tank, the approximate time required for the solution was 35 msec using serial arithmetic unit, and 10 msec using sequential arithmetic unit.

With a random-access memory, the solution times were approximately 32 milliseconds using the serial arithmetic unit and 8.4 milliseconds using the sequential arithmetic unit. It can be seen that the use of the NSF unit in conjunction with the serial memory permitted better than 90 per cent of perfect minimum access programming to be attained with the serial arithmetic unit and better than 80 per cent to be attained with the sequential arithmetic unit.

Adding the time required for the input and output operations it was seen that the computer using the serial arithmetic unit was *just* able to perform the complete solution in the prescribed time interval of 50 milliseconds, while the computer using the sequential arithmetic unit was able to perform the solution in less than one-third of the required time. Both were able, therefore, to solve the stated problem in real-time.

The computer described here (with either type of arithmetic unit) can be constructed with conventional OR-AND-OR pyramid circuits such as are used in the SEAC. Detailed logical design of the computer using this type of circuitry indicates that the amount of equipment involved is about the same as that in a general purpose computer of twice its precision (such as the SEAC).[6] If a random access memory is to be used with the sequential unit, it must be capable of repetitive consultations every 5 microseconds.

Acknowledgment

The authors gratefully acknowledge the suggestions of Dr. Harry J. Gray, Jr., Dr. Morris Rubinoff and Gerald R. Songster of the Moore School of Electrical Engineering, University of Pennsylvania.

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A Diode Multiplexer for Analog Voltages*

H. J. GRAY, JR.†, M. RUBINOFF†, AND J. TOMPKINS†

Summary—A diode multiplexer switch is described for time-sharing 64 analog voltages in a digital computer application. Apart from its relative simplicity and economy, the multiplexer characteristics of microsecond switching speeds, maximum settling time of 133 microseconds for a 10-volt operating range, and accuracies of better than 1 per cent full scale are confirmed both by theoretical equations and by experimental results.

Introduction

A MULTIPLEXER is a switching device for connecting any one of a number of wires to a single wire. For example, when a number of analog voltages are to be transmitted over a single wire to a number of remote points, a "many-to-one" multiplexer is used to connect each voltage in its turn to the near end of the wire, and a "one-to-many" multiplexer is used to connect the far end of the wire to the remote points one at a time. A single-pole multiposition switch is clearly a primitive multiplexer, and when used within its limitations, a highly effective one.

In the design of a digital real-time simulator[1] it proved advantageous to provide for the conversion of many digital signed magnitudes into analog voltages. It was proposed to do this by time-sharing one digital-to-analog converter by using a multiplexing device.

The requirements to be fulfilled by the multiplexer in question were as follows:

1. Simplicity sufficient to assure economical multiplexing of 64 voltages;
2. Speed sufficient to serve as a component in a real-time simulator. 100 microseconds was set as a goal for switching time;
3. Accuracy of at least 1 per cent of full scale with zero drift not to exceed 0.1 per cent per hour;
4. Compatibility with other simulator components, such as the computer gating circuits and instrument servoamplifiers serving as output loads.

Existing multiplexing switches were investigated,[2–5] none of which was satisfactory for the application either because of high degree of complexity or insufficient accuracy. On the other hand, the diode multiplexer described in this paper proved to be a satisfactory answer to the problem. It bears a close resemblance to a bi-directional switch, used in a different application.[6] Static characteristics of a number of similar structures are discussed elsewhere.[7]

Description of Multiplexer

The system as used is diagramed in Fig. 1. The operation of the multiplexer can be better understood by reference to Fig. 2, which is derived from Fig. 1 by a horizontal bisection along a line joining input to output.

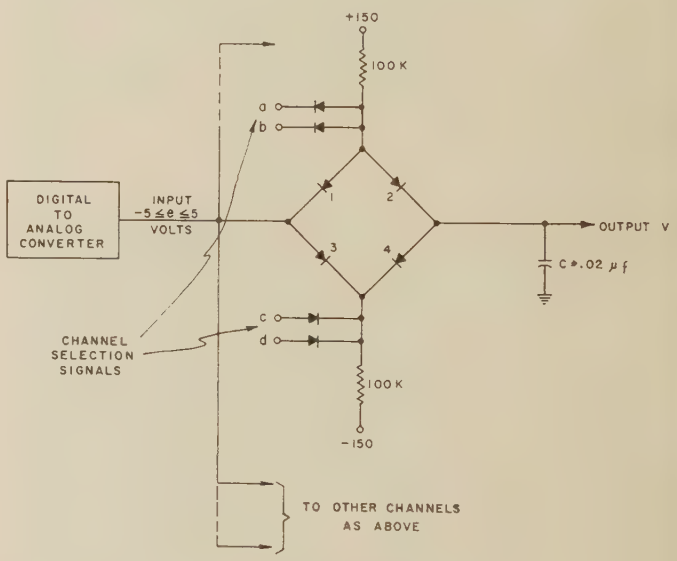

Fig. 1—Multiplexing system.

Assume that $-5 \leqq e \leqq 5$ volts, $-5 \leqq v \leqq 5$ volts, and $a, b < -5$ volts, $c, d > 5$ volts. Then 1–4 are nonconducting. The charge on capacitor C will leak off through the reverse impedance of diodes 1 and 4. In the digital real-time simulator under consideration, C is recharged through the multiplexer at 50 millisecond intervals. Based on leakage figures for silicon junction diodes ($< 10^{-8}$ amperes at -10 volts) and allowing for the amplifier load on the output, leakage current does not exceed 4×10^{-8} amps. (Note in Fig. 1 that the diode leakage currents oppose one another.) To assure less than 0.1 v drift (1 per cent) due to leakage, it is required that

$$C \geqq \frac{I\Delta t}{\Delta V} = \frac{4 \times 10^{-8} \times 50 \times 10^{-3}}{0.1} = 2 \times 10^{-8}.$$

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Note further that the circuit in Fig. 2 (a) is a positive "AND" circuit and Fig. 2 (b), a negative "AND" circuit. Hence if *a and b* are raised above 5 volts, V will rise to a value slightly exceeding e. Similarly, when *c and d* are lowered below -5 volts, V will fall to a value slightly below e. Thus, in Fig. 1, if a and b exceed 5 volts, and c and d are below -5 volts, V will assume a value almost equal to e.

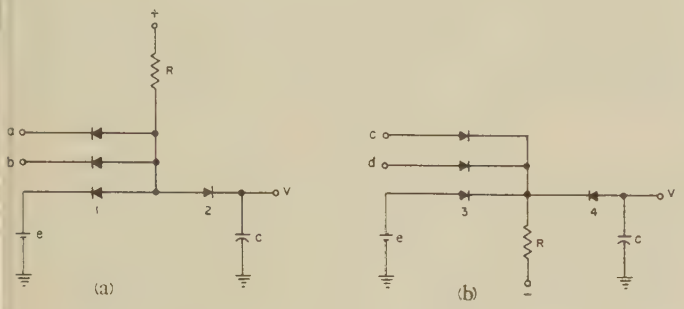

Fig. 2—Derivation of diode bridge.

Both halves of the multiplexer are needed. The half shown in Fig. 2 (a) charges the condenser C when v is initially below e; the half shown in Fig. 2 (b) discharges C when v is initially above e.

Since the multiplexer is derived from conventional gating circuits used in digital computers, some of the gating needed to select a specific instrument can be performed within the multiplexer. A double coincidence selection system has been assumed for the preceding.

Determination of Switching Time

The selection of a new channel is followed by an interval during which v makes the transition to voltage e. An approximate determination of this interval will now be obtained in closed form.

A silicon junction diode such as the 1N138A has a forward voltage-current characteristic such that in the range of interest $i=\beta \exp \alpha v$ where β and α are constants. This is quantitatively correct for the forward characteristic of the 1N138A if $\alpha=26.5$ and $\beta=6.25\times 10^{-12}$. The same equation may be extended to apply to the reverse characteristic in that both the true reverse current and the current given by the exponential function are negligible.

Consider the simplified equivalent circuit in Fig. 3. The input voltage is assumed for simplicity to be zero. This does not incur any loss of generality. All diodes have been assumed identical for the analysis.

The circuit equations are

$$\begin{aligned} C dv/dt + \beta \exp [\alpha(v - v_2)] - \beta \exp [\alpha(v_1 - v)] &= 0 \\ \beta \exp [\alpha(v_1 - v)] + \beta \exp [\alpha v_1] &= I \\ \beta \exp [\alpha(v - v_2)] + \beta \exp [-\alpha v_2] &= I \\ \beta \exp [-\alpha v_2] - \beta \exp [\alpha v_1] &= i_1. \end{aligned} \tag{1}$$

The second and third equations of (1) may be substituted into the first and fourth equations to yield, after rearrangement,

$$C dv/dt = -I \tanh (\alpha v/2) \tag{2}$$

$$i_1 = -\tanh (\alpha v/2). \tag{3}$$

We are concerned only with those cases when v_0, the initial value of v, is of the order of 1 volt. Then $\alpha v_0 \gg 1$, $\sinh \alpha v_0 \approx -\frac{1}{2} e^{-\alpha v_0}$, and (2) has the solution

$$v \approx (2/\alpha) \sinh^{-1} \{(1/2) \exp [-\sigma(t - t_0)]\}, \tag{4}$$

where $\sigma = \alpha I/2C$ and $t_0 = Cv_0/I$.

Case 1: $t \leqq t_0$

For $t<t_0$, except for values of t very close to t_0, a good approximation of $\sinh^{-1}$ may be had by keeping only the first term of the expansion

$$\sinh^{-1} x = \log 2x + \frac{1}{2.2x^2} - \cdots ; x > 1. \tag{5}$$

Hence

$$v \approx v_0 - It/C; t < t_0, v_0 > 0. \tag{6}$$

This corresponds to the interval when only diodes 1 and 4 are conducting.

Case 2: $t=t_0$

For $t=t_0$, (4) becomes

$$v(t_0) = (2/\alpha) \sinh^{-1} (1/2) = 0.962/\alpha.$$

This is only 0.0364 volts for the 1N138A.

Case 3: $t>t_0$

Here it yields a good approximation to keep the first term of the power series expansion of $\sinh^{-1}$. Hence

$$v \approx (1/\alpha) \exp [-\sigma(t - t_0)]; t > t_0, v_0 > 0. \tag{7}$$

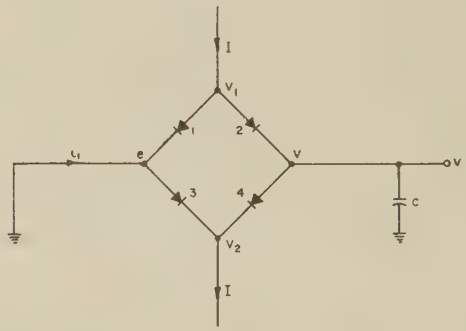

Fig. 3—Equivalent circuit.

The decay time constant for the values in Fig. 1 is $1/\sigma=1\mu$s. The value of t_0 is correspondingly 133 μs for a 10-volt change. These values were satisfactory.

From (3), the following approximations are evident

$$\begin{aligned} i_1 &\approx -I; t < t_0 \\ i_1 &= -0.447I; t = t_0 \\ i_1 &\approx -(I/2) \exp [-\sigma(t - t_0)]; t > t_0. \end{aligned} \tag{8}$$

Equivalent circuits derived from (6), (7), and (8) are given in Fig. 4 for the case when the generator has an internal resistance, R_g.

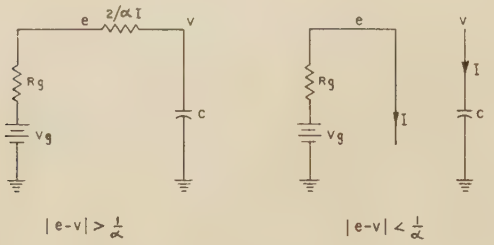

Fig. 4—Equivalent circuits.

Although the last of (8) implies that i_1 goes to zero, this is not usually so, as demonstrated for a multiplexing switch in steady state (Fig. 5). Solution of the nodal

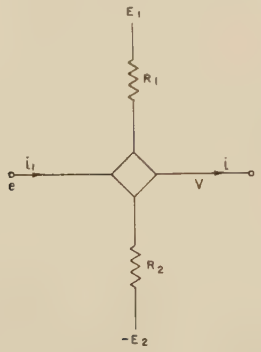

Fig. 5—Equivalent circuit in steady-state.

equation for this circuit yields

$$i_1 = i + e\left[\frac{1}{R_1} + \frac{1}{R_2}\right] + \frac{E_2}{R_2} - \frac{E_1}{R_1}.$$

Note there is a current offset $i + E_2/R_2 - E_1/R_1$ and an effective input resistance $R_1R_2/(R_1+R_2)$.

The static error that results when the diodes are not perfectly matched can be estimated. The steady-state equations of Fig. 3 may be solved to yield

$$v \approx (v_0/2\alpha)(-\alpha_1 + \alpha_2 + \alpha_3 - \alpha_4) + (1/2\alpha\beta)(-\beta_1 + \beta_2 + \beta_3 - \beta_4) + \cdots, \quad (9)$$

where v_0 is such that $I/2 = \beta \exp(\alpha v_0)$.

For $v_0 = 0.7$ volts and $\alpha = 26.5$, which are reasonable values for silicon diodes in the present application, (9) becomes

$$|v| \leqq 1.4a + 0.07b,$$

where a and b are the maximum anticipated per cent variations in α and β, respectively.

Experimental Results

The diode multiplexer circuit was breadboarded using four unmatched 1N100 germanium diodes in the multiplexer bridge. Despite the random choice of diodes the error voltage between e and v was less than 0.05 volt over the ± 5-volt range.

The switching time to swing the output over the full range of 10 volts was found to be 125 μs. This was measured by applying a 10-volt $p-p$ sine wave to the input and observing on an oscilloscope the frequency (4 kc) at which the triangularly-shaped output wave initially became attenuated.

Conclusion

A multiplexing switch has been described which is relatively inexpensive, which is capable of achieving accuracies of 1 per cent of full scale or better, has low drift, and is microsecond fast. The only fundamental limitations on the speeds that might be achieved seem to be the diode capacitance and recovery time, which for the silicon diodes in the system described were respectively about 10 $\mu\mu$f and 1 μs.

Acknowledgment

The authors are very grateful to Mrs. E. L. Fishl who typed the manuscript.

Some Notes on Logical Binary Counters*

R. M. BROWN†

Summary—The properties of binary counters which utilize non-transient storage elements for the count information are presented. The four possible sets of logical connections between the two storage elements necessary for each stage are described. The binary numbers represented in the storage elements are shown to be the actual count in one set of elements and in the other set a Gray code representation of twice the actual count. Examples of bi-directional counters are given.

Introduction

IN THE TRANSFER of information in digital computing machinery, a design philosophy of widespread application[1] requires semi-permanent storage of the information at all times during the transfer. In practice, this involves two separate sets of time independent storage elements such as flip-flops, one of which holds and transmits the information to the other during any transfer so that the second or receiving set is the only one undergoing change of state. This philosophy necessarily excludes the use of capacitors as information storage elements because of the transient nature of their storage. The increased circuit complexity resulting is usually justified by the freedom from timing difficulties and the resultant greater reliability.

A specific application of this principle occurs in the design of circuits for binary counting. Here the present count value must be stored in one set of storage elements while the next count is prepared in a second set. Methods for achieving this were recently described by Ware.[2] It is the purpose of this paper to consider further the complete set of logical connections available and thus to explain the behavior of the counting elements.

The Counting Action

A consideration of the sequence of numbers occurring in a binary count reveals that, for positive or additive counting, a binary digit at any point must reverse its value when and only when the next lower digit in the counter undergoes a change from a *1* to a *0*. Similarly for negative or subtractive counting, the reversal occurs when the next lower digit changes from a *0* to a *1*. Then it is necessary only for the logical circuitry associated with each binary stage to sense those particular changes in the state of the previous stage and to produce a reversal of the digit presently held. The input or actuating signal to the counter may consist of a signal simulating a previous stage changing from *0*'s to *1*'s and back again.

The design philosophy described above determines the methods by which the reversal of a digit is accomplished. Each binary stage contains two flip-flops or toggles called the True and the False rank toggles using the notation of Ware,[2] and also the logical circuitry to gate between these toggles so as to produce a digit reversal at the appropriate time in the count. The complete set of True toggles represents the actual binary count value. The False rank toggles contain a number representative of, but not identical with, either the previous or next count value, depending on whether one is concluding or initiating a count action. The counting sequence within each stage is determined by gating operations between the True and False toggles of that stage; the gates, in turn, are controlled by the contents of the previous stage.

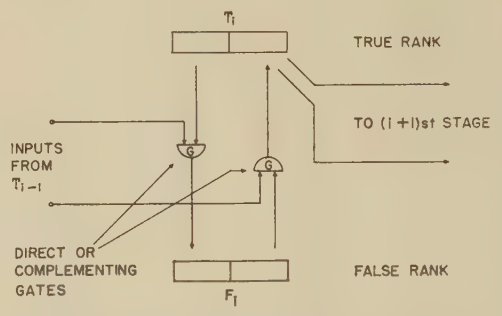

Fig. 1—Schematic drawing of the gating connections to the True and False toggles of a single stage of a logical binary counter.

Fig. 1 shows a schematic drawing of the gating connections for one stage of a binary counter of this type. The gates between the True and False toggles are indicated only in a general fashion inasmuch as the particular gating rules used determine which of the two gate transfers contains the complementation action necessary to produce reversal. Table I indicates the two possible

TABLE I

Gating Rules for Logical Binary Counters*

	Adding counters	Subtracting counters
Set No. 1		
If $T_{i-1} = 0$	$F_i \xrightarrow{c} T_i$	$T_i \xrightarrow{c} F_i$
1	$T_i \rightarrow F_i$	$F_i \rightarrow T_i$
Set No. 2		
If $T_{i-1} = 0$	$F_i \rightarrow T_i$	$T_i \rightarrow F_i$
1	$T_i \xrightarrow{c} F_i$	$F_i \xrightarrow{c} T_i$

* The symbolism $T \xrightarrow{c} F$ indicates that the contents of the True toggle are complemented in transfer to the False toggle.

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[1] This philosophy originated with the Computer Group at the Institute for Advanced Study and has since been adopted on all machines of the IAS type. See W. H. Ware, Proc. IRE, vol. 41, pp. 1429–1447; October, 1953.

[2] Ware, *ibid.*

sets of gating rules for transfers from True to False toggles and vice versa, which result in either an additive or subtractive count. The difference in the two basic sets is determined by which direction of transfer contains a complementation. Set No. 1 gives the rules treated by Ware; Set No. 2 gives the other possible combination suggested but not treated by Ware.

Table II shows the binary numbers held in the True and False rank toggles for both additive and subtractive counters of three-digit capacity. Each count requires two disjunctive input signals into the lowest stage of the counter; therefore, the toggle values for both the True and False ranks are shown for each half-count.

TABLE II
TRUE AND FALSE RANK NUMBERS FOR LOGICAL BINARY COUNTERS

Count	Toggle	Set No. 1 Gating Rules		Set No. 2 Gating Rules	
		Additive	Subtractive	Additive	Subtractive
0	True	000	000	000	000
	False	111	111	000	000
½	*T*	000	111	000	111
	F	110	111	001	000
1	*T*	001	111	001	111
	F	100	110	011	001
1½	*T*	001	110	001	110
	F	101	100	010	011
2	*T*	010	110	010	110
	F	001	101	110	010
2½	*T*	010	101	010	101
	F	000	001	111	110
3	*T*	011	101	011	101
	F	010	000	101	111
3½	*T*	011	100	011	100
	F	011	010	100	101
4	*T*	100	100	100	100
	F	011	011	100	100
4½	*T*	100	011	100	011
	F	010	011	101	100
5	*T*	101	011	101	011
	F	000	010	111	101
5½	*T*	101	010	101	010
	F	001	000	110	111
6	*T*	110	010	110	010
	F	101	001	010	110
6½	*T*	110	001	110	001
	F	100	101	011	010
7	*T*	111	001	111	001
	F	110	100	001	011
7½	*T*	111	000	111	000
	F	111	110	000	001
0	*T*	000	000	000	000
	F	111	111	000	000

It can be seen that the False rank numbers for the two sets of gating rules and for a given counter type (e.g., additive) are the *1*'s complements of each other. This results from the fact that the complementation upon gating occurs in opposite directions of transfer for the two sets. Furthermore, the False rank numbers for the Set No. 2 counters are simply the reflected binary or Gray code[3] for binary counting at a rate twice that of the actual count. The explanation for this lies in the basic principle of counting by this logical method.

The True or False toggles of a given stage can be changed only by the opening of a gate from the opposite toggle of that stage. This gating operation is initiated by the change of the True toggle of the previous stage. In other words, until the True toggle of the previous stage changes its value from a *1* to a *0* or vice versa, there can be no change of gating in the stage and thus no change in either the True or False toggles of that stage. From this it follows that during a given half-count, the counting action, producing changes of gating direction, will propagate from the input stage up to the first stage at which a True to False gating is initiated. At this point no change in that True toggle can occur and thus no change in gating conditions can be transmitted to higher stages. This behavior permits one and only one True to False gate per half-count. Furthermore, because of the complement gating in only one direction within each stage, the value of the False toggle of any stage is changed with each True to False gate of that stage. From this we see that only one False toggle can change during a half-count; and one such change must occur for each half-count except for those which propagate action to the end of the counter—i.e., which would initiate False to True gates at the highest stage. The latter case corresponds to an overflow of False count at the end of the counter; thus no False count toggle changes. Since the property of counting with one toggle change per count is peculiar to a Gray method of binary counting, this characteristic of the False rank numbers is explained.

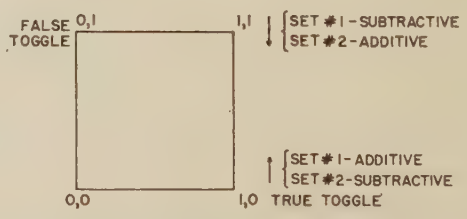


Fig. 2—Geometric picture of the sequence of toggle values traversed in the counting action of a single counter stage.

A simple picture of the difference between the two sets of gating rules is illustrated in Fig. 2. Taking the binary values of the True and False toggles as defining points in a plane, the action for a single stage in counting through the sequence of values *0* to *1* to *0* may be indicated by the traversal of the square. Set No. 1 gating

[3] F. Gray, "Pulse Code Communication," Patent 2,632,058; March 17, 1953.

rules result in a counterclockwise traversal for additive counters and a clockwise traversal for subtractive; Set No. 2 gating rules produce reversed directions of traversal.

Applications

A simple bi-directional counter may be constructed by using those gating rules of Sets No. 1 and No. 2 which have the same direction for complementation (e.g., Set No. 1 for adding, and Set No. 2 for subtracting). An externally controlled switch is provided at each stage to interchange the information from the previous True toggle which actuates the gates. Consider, for example, the gating rules:

$$F_i \xrightarrow{c} T_i \qquad (1)$$

$$T_i \rightarrow F_i. \qquad (2)$$

If $T_{i-1}=0$ actuates (1), and $T_{i-1}=1$ actuates (2), the count action will be additive. A reversal of connections to the previous stage produces a subtractive counter. A similar arrangement can be made with those gating rules which complement on the True to False transfer.

TABLE III

Gating Rules for a Bi-Directional Counter

If have T_{i-1}	F_{i-1}	*Gating Set No. 9*	
0	1	$F_i \xrightarrow{c} T_i$	Direction for positive count
0	0	$T_i \xrightarrow{c} F_i$	
1	0	$T_i \rightarrow F_i$	
1	1	$F_i \rightarrow T_i$ ↓	
		Gating Set No. 2	
0	0	$F_i \rightarrow T_i$	Direction for positive count
0	1	$T_i \rightarrow F_i$	
1	1	$T_i \xrightarrow{c} F_i$	
1	0	$F_i \xrightarrow{c} T_i$ ↓	

A considerably more complicated but quite useful bi-directional counter[4] may be constructed by combining gating rules and using the values of both the True and False toggles of the previous stage to actuate gates. In this case two separate double-valued input signals are required, and the count action becomes a four-step process. Table III gives the gating rules for the two such counters; Table IV gives the True and False rank numbers for such a counter of four using Gating Set No. 2. The input signals shown represent the signals on the two lines into the first stage necessary to actuate the counting. It is seen that the actual toggle values change only every half-count and not every $\frac{1}{4}$ count. It is necessary, however, to receive each $\frac{1}{4}$ count at the input in order to establish the direction of counting. To reverse the direction of counting, the sequence of input signals is traversed in the opposite sense. This counter will count reversably and unambiguously provided that the order of input signals is reversed but not permuted.

[4] The concept for this counter arose from discussions with Mr. Howard Knoebel of the Control Systems Laboratory concerning a relay circuit to perform similar functions.

TABLE IV

True and False Rank Numbers for Counting from 0 to 2 and Back to 0 for a Bi-Directional Counter

Positive Direction				Negative Direction			
Count	Toggle	Number	Input	Count	Toggle	Number	Input
0	*T*	00	0	2	*T*	10	0
	F	00	0		*F*	10	0
$\frac{1}{4}$	*T*	00	0	$1\frac{3}{4}$	*T*	01	1
	F	00	1		*F*	10	0
$\frac{1}{2}$	*T*	00	1	$1\frac{1}{2}$	*T*	01	1
	F	01	1		*F*	10	1
$\frac{3}{4}$	*T*	00	1	$1\frac{1}{4}$	*T*	01	0
	F	01	0		*F*	11	1
1	*T*	01	0	1	*T*	01	0
	F	11	0		*F*	11	0
$1\frac{1}{4}$	*T*	01	0	$\frac{3}{4}$	*T*	00	1
	F	11	1		*F*	01	0
$1\frac{1}{2}$	*T*	01	1	$\frac{1}{2}$	*T*	00	1
	F	10	1		*F*	01	1
$1\frac{3}{4}$	*T*	01	1	$\frac{1}{4}$	*T*	00	0
	F	10	0		*F*	00	1
2	*T*	10	0	0	*T*	00	0
	F	10	0		*F*	00	0

A useful application of this counter lies in the determination of the position of a shaft which may reverse its direction of motion. A disk with two sets of overlapping slots and two photocells and light sources can provide the sequence of the two counting signals into the input of the lowest stage in a manner analogous to the signals from the True and False toggles of a previous stage. The direction of rotation of the shaft directly determines the direction of counting; there are no ambiguous shaft positions or combinations of motions which can confuse the counter. The accuracy is determined by the slit sizes and the optical arrangement.

A Variable Binary Scaler*

D. B. MURRAY†

Summary—The binary elements of a counter or "scaler" may be interconnected in many ways. This paper discusses a class of interconnections in which some elements are "forward-counting" and some are "reverse-counting." By changing the interconnections any arbitrary integral scaling ratio (up to the counter capacity) may be obtained.

Introduction

THE FAMILIAR FLIP-FLOP principle has followed three basic lines of development: first, the extension of the principle to include not only the original vacuum-tube pairs, but also relays, transistors, thyratrons, cold-cathode gas tubes, and externally-stabilized neon glow tubes;[1] secondly, the improvement of these various circuits, especially with regard to stability, speed of operation, and ease of triggering; and, thirdly, the application of the many types of flip-flops to computing, scaling, time measurement, and other functions involving some form of pulse counting. The present discussion deals with one of these functions: scaling. It will treat the flip-flop circuits in their most general form, using only block diagrams, so that the principles of operation may be applied to any of the presently-existing flip-flop forms.[2]

Types of Counters and Scalers

Scalers of fixed scaling ratio have limited application. In their most familiar form, they appear as decade scalers, or scalers whose ratio is fixed at some value 2^n. To increase the usefulness of scalers, many kinds of circuits have been devised to give an integral, variable scaling ratio. The method of achieving variability differs with the type counter used as the basic circuit. However, counters have, in general, taken two forms: those based on multi-stable circuits, and those based on bi-stable circuits. Among the multi-stable circuits there are, for example, "ring" counters, and tri-stable "flip-flops." In a ring counter, out of n triodes (or thyratrons, cold-cathode tubes, etc.) only one can conduct, while n-1 are blocked—and this ring has n stable states. Among the bi-stable circuits are flip-flop rings (in which only 1 out of n flip-flops can be "on" at any one time), and flip-flop binary counters. Both ring counters (usually decade rings) and binary counters have been used for scaling circuits; and both have been applied to variable scalers. The binary counter has wider appeal for this application, because, having fewer tubes, it is considerably more economical; and, for the same reason, it has a lower input electrostatic capacity, which permits higher operating speeds.

In the case of ring counters, variability of scaling ratio is quite simple, being achieved by taking the output from any desired tube in the ring. In the case of binary counters, a method of presetting and forced resetting has been used.[3] In this method, if a counter of maximum capacity n (decimal notation) is used, and a scaling ratio, r (decimal notation) is desired, the counter is preset to $n-r$, so that pulse $r-1$ sets the counter to maximum capacity, and pulse r returns the counter to 0, producing the desired output pulse. This output pulse is then passed through a variable network which directs it to the proper flip-flops for resetting the counter to $n-r$. The network also converts $n-r$ from decimal to binary notation. Another method of obtaining a variable scaling ratio with a binary counter is described in the following paragraphs.

Principle of Operation

The circuit is based on a combination of forward-acting and reverse-acting binary counters. Fig. 1 shows a normal, forward-acting counter. It is assumed that the

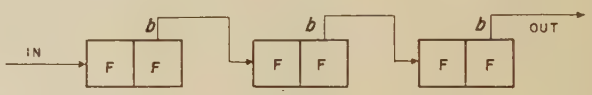


Fig. 1—Forward-acting binary counter.

normal or *off* (0) condition of any flip-flop is with the right-hand tube conducting; that the *on* (1) condition is with the left-hand tube conducting; and that a change of state will occur whenever a *negative* pulse appears at the input lead of a flip-flop. The operating sequence of the circuit of Fig. 1 is:

000 100 010 110 001 101 011 *111* *000*.

(The meaning of the italics will be explained below.)

Fig. 2, on the facing page, shows a reverse-acting counter.[4] The operating sequence is:

000 111 011 101 *001* *110* 010 100 000.

That the operating sequence is such can be understood by observing that a negative pulse appears on the *a*-lead whenever a flip-flop changes from the *off*-condition to the *on*-condition; whereas a negative pulse appears on the *b*-lead, when it changes from the *on*-condition to

* Original manuscript received, September 3, 1954; revised manuscript received, January 28, 1955.

† Woodstock College, Woodstock, Maryland.

[1] The reader will be familiar with most of the many developments and modifications of different kinds of trigger circuits. Attention is called to the neon glow tube flip-flop. Cf. U. S. Patent No. 2,604,589, issued to Meryl C. Burns; July 22, 1952.

[2] The exception to this would be certain types of trigger circuits using a single point-contact transistor.

[3] H. Lifshutz, "New vacuum tube scaling circuits of arbitrary integral or fractional scaling ratio," *Phys. Rev.*, vol. 57, pp. 243–244; 1940. J. J. Wild, "Predetermined counters," *Electronics*, vol. 20, pp. 121–123; March, 1947. R. J. Blume, "Predetermined counters for process control," *Electronics*, vol. 21, pp. 88–93; February, 1948.

[4] R. L. Trent, "A Transistor Reversible Binary Counter," *Nat. Electronics. Conf. Proc.*, vol. 8, pp. 346–357; 1952.

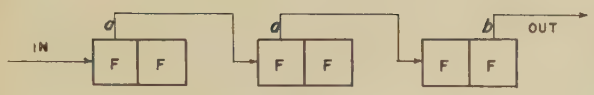


Fig. 2—Reverse-acting binary counter.

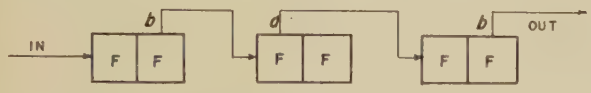


Fig. 3—A combination of forward-acting and reverse-acting elements.

the *off*-condition. The first input pulse changes the first flip-flop from 0 to 1, producing an output pulse on the *a*-lead. This pulse changes the second flip-flop from 0 to 1, which also produces an output pulse on the *a*-lead, changing the third flip-flop from 0 to 1. This type counter is used in an accumulator-type computer for subtraction.

These two methods of interconnecting the flip-flops are obviously not the only possible ones. Figs. 3 and 4 show two other combinations. The operating sequences are respectively:

000	100	011	111	001	*101*	*010*	110	000
000	110	010	101	001	111	*011*	*100*	000.

Since a negative pulse will appear on the *b*-lead of the last flip-flop in the chain whenever that flip-flop changes from 1 to 0, it follows that an output pulse will appear in the circuit of Fig. 1 on the 8th pulse; in the circuit of Fig. 2 on the 5th pulse; in the circuit of Fig. 3 on the 6th pulse; and in the circuit of Fig. 4 on the 7th pulse—as indicated by the italics in the operating sequences listed above. This output pulse is also used to reset or clear the counter to 000, as indicated in Fig. 5. This same figure adds two switches by which the interconnections—and, therefore, the scaling ratio—may be varied. The method of feedback and resetting will, of course, depend on the type flip-flop used.

Fig. 4—A combination of reverse-acting and forward-acting elements in that order to produce another combination different from that of Fig. 3.

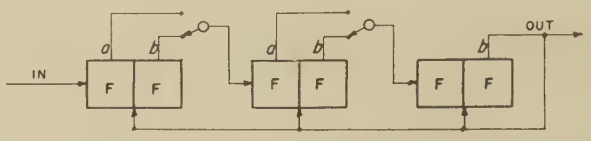


Fig. 5—A counter with switches to change the interconnections and with a connection for resetting to 000.

There are still four more scaling ratios possible with the circuits of Figs. 1 to 4, for the output lead can be connected to the *a*-lead of the last flip-flop in the chain, instead of to the *b*-lead as shown in these figures. If this is done, there will be no change in the operating sequences of the circuits, but there will be a change in the output pulse. Instead of appearing at the output lead when the last flip-flop changes from 1 to 0, it will appear when the last flip-flop changes from 0 to 1. This will take place in Fig. 1 when the 4th pulse appears at the input lead; in Fig. 2 when the 1st pulse appears; in Fig. 3 when the 2nd pulse appears; and in Fig. 4 when the 3rd pulse appears. As in the former cases, the output pulse is used to reset the scaler to 000. If, then, a switch replaces the output lead of Fig. 5, there is had a scaler of variable scaling ratio from 1 to 8.

The correct switch connections for a given scaling ratio will be: *aaa*, *baa*, *aba*, *bba*, *aab*, *bab*, *abb*, *bbb*—as the ratio increases from 1 to 8. This progression is easily seen to be itself of a binary-code nature.

Practical Circuits

Fig. 6 (next page) is a circuit with a scaling ratio variable from 1 to 16. Relays have been substituted for the switches of Fig. 5. Table I shows the operating se-

TABLE I

Interconnections and Operating Sequences for the Circuits of Figs. 6 and 8

Scale	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
Conn.	*aaaa* 0000	*baaa* 1000	*abaa* 0100	*bbaa* 1100	*aaba* 0010	*baba* 1010	*abba* 0110	*bbba* 1110	*aaab* 0001	*baab* 1001	*abab* 0101	*bbab* 1101	*aabb* 0011	*babb* 1011	*abbb* 0111	*bbbb* 1111	
0	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0000	0
1	1111	1000	1100	1000	1110	1000	1100	1000	1111	1000	1100	1000	1110	1000	1100	1000	1
2		0111	0100	0100	0110	0110	0100	0100	0111	0111	0100	0100	0110	0110	0100	0100	2
3			1011	1100	1010	1110	1010	1100	1011	1111	1011	1100	1010	1110	1010	1100	3
4				0011	0010	0010	0010	0010	0011	0011	0011	0011	0010	0010	0010	0010	4
5					1101	1010	1110	1010	1101	1011	1111	1011	1101	1010	1110	1010	5
6						0101	0110	0110	0101	0101	0111	0111	0101	0101	0110	0110	6
7							1001	1110	1001	1101	1001	1111	1001	1101	1001	1110	7
8								0001	0001	0001	0001	0001	0001	0001	0001	0001	8
9									1110	1001	1101	1001	1111	1001	1101	1001	9
10										0110	0101	0101	0111	0111	0101	0101	10
11											1010	1101	1011	1111	1011	1101	11
12												0010	0011	0011	0011	0011	12
13													1100	1011	1111	1011	13
14														0100	0111	0111	14
15															1000	1111	15
16																0000	16
Output in		ff 1	ff 2	ff 2	ff 3	ff 3	ff 3	ff 3	ff 4	ff 4	ff 4	ff 4	ff 4	ff 4	ff 4	ff 4	

quences of this circuit for various values of scaling ratio. At the top of the chart are the interconnections required to obtain the desired ratio. For example, if the scaling ratio is to be 5, the interconnections must be *aaba*—that is, the second flip-flop is connected to the *a*-lead of the first; the third is connected to the *a*-lead of the second; the fourth to the *b*-lead of the third; and the output and resetting pulse is obtained from the *a*-lead of the fourth. Connections to any *a*-lead are had when relays are unenergized (0), and to any *b*-lead when they are energized (1). Therefore the letters at the top of the chart can be changed to the conventional binary code, as has been done in the second line.

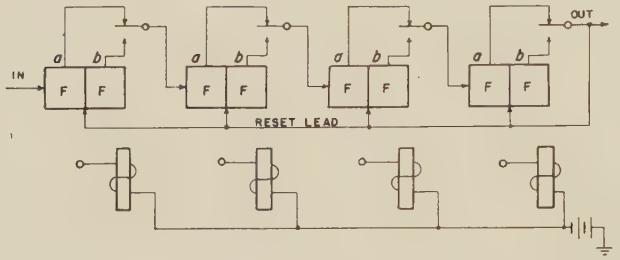


Fig. 6—A counter with four flip-flops showing relays to change the scaling ratio.

The value of the binary sequence of interconnections is not so apparent in the circuits of Fig. 6 as in those of Fig. 7. It is true that relay circuits can be designed to operate in binary sequence, but this is not usually done. In Fig. 7, the relays have been replaced by electronic gates, controlled by a second flip-flop binary chain. The scaling ratio, in the form of a series of pulses, can be fed into the control counter, which, in its turn, opens or closes the gates required to give the operating sequence for that particular ratio.

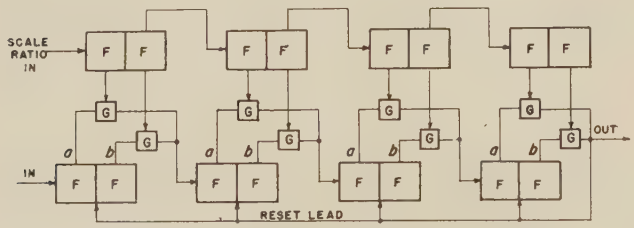


Fig. 7—A variable scale counter with electronic switches controlled by a second counter.

One caution must be observed in this connection. The binary number in the control counter does *not* correspond to the scaling ratio required, but is one *less* than that ratio. Thus, for example, if a scaling ratio of 5 is required, the proper interconnections are *aaba*—or 0010 in binary notation—which is 4, not 5, in the decimal system.

There are two possible solutions to this difficulty. The first and most obvious is to reset the control counter in such wise that its 0-setting is 1111, and not 0000. In this case, the first pulse of the scaling ratio series will advance the counter to 0000, the second pulse to 1000, the third to 0100, etc.—which are the proper codes for ratios of 1, 2, 3, etc. In the second method, the control counter is connected as a reverse-acting counter (as described above). Therefore its operating sequence will be 0000, 1111, 0111, 1011, 0011, 1101, 0101, 1001, 0001, 1110, 0110, 1010, 0010, 1100, 0100, 1000, 0000. Now, if the connections to the relay contacts (or gates) are reversed so that an energized (1) relay connects *a*-leads, and an unenergized (0) relay connects *b*-leads, the required interconnections will be made—i.e., the first pulse changes the control counter to 1111 (*aaaa*), the second pulse to 0111 (*baaa*, etc.).

Actually these are not two different methods, but the same method. It really comes down to a question of definition. It is, however, better to define on-and-off, *a*-and-*b* in the second way, because then all the relays will be unenergized in their "off" or normal state (before any pulses are applied), whereas in the first case the "off" state is with all relays energized. Where flip-flops and gates are used for control, it would not seem to make any difference.

Table I can be extended for scaling ratios up to 32, 64, 128, etc., by noting the regularly recurring patterns. However, this is not necessary, for it will be found that the only requirement is the addition of flip-flop stages, their interconnections following the same binary sequence as that of the four-stage scaler.

There may be applications where it is desirable to obtain the output pulse from a *b*-lead at all times, regardless of the scaling ratio used. A further examination of the chart of Table I indicates how this may be done. The last line of the chart, marked "output" indicates the flip-flop from which the output and resetting pulse is taken. The logic of this is easily seen by examining the various operating sequences, keeping in mind that when the flip-flop changes from its "on" condition (1) to its "off" condition (0), a negative pulse appears on the *b*-lead of that flip-flop.

Interpretation of the Intermediate States

When binary counters are modified for variable scaling using the methods just outlined, then the intermediate states are not easily interpreted because the resulting binary code is not the usual simple one. This is true of the scaler just described. For example, consider a scaling ratio of 9. Table I shows that the second pulse will set the counter to 0111, which is 14 (rather than 2) in the decimal system. However, for many applications, a knowledge of the intermediate states is not required; as, for instance, when the scaler is used for "scaling down" pulse rates for magnetic counters, or when it is used as a time-base generator.

It is not impossible to interpret the intermediate states with this circuit, because obviously there is a unique circuit combination for any condition of scaler, control circuit, and input pulse number. Extra contacts on the relays can be used in various combinations of logical "and" circuits to represent this unique condition.

This is somewhat complicated, but not as much as would appear at first glance. Reference to the chart shows that any input pulse is represented by only three or four possible code positions, with the exception of the 3rd input pulse, which can be represented by any one of five code positions. Thus, for example, the 5th input pulse can be represented by the binary equivalent of 5, 7, 11, or 15.

Sometimes it is necessary to know the value of the number in one of the counting steps only to determine whether the number is larger or smaller than some other number. When this is the case, a means for "automatic" interpretation is available. In division, this would be called "rounding off."

To understand the method, consider that the scaler is being used as a divider: a certain number of pulses, representing the dividend, is fed into the scaler; the scaling ratio represents the divisor; and a certain number of output pulses represents the quotient. Two cases will be considered: that in which the units place is to be rounded off, and that in which the quotient is to be carried out to one (or more) decimal places and then rounded off. For the purpose of illustration, the usual—though somewhat inaccurate—convention is adopted: 0.5 or greater adds 1 to the quotient, while 0.4 or smaller is dropped from the quotient.

First Case

If 7 is to be divided by 2, the quotient will be $3\frac{1}{2}$, which rounds off to 4. Therefore the scaling ratio is set for 2, and 7 pulses are fed into the scaler. The input pulses that produce output pulses will be the 2nd, 4th, and 6th, giving a quotient of 3, which is incorrect. But, if 1 pulse is fed into the scaler before the arrival of the chain of 7 pulses, output pulses will be obtained for the 1st, 3rd, 5th, and 7th input pulse, giving the correct quotient, 4.

Suppose it is desired to divide 9 by 3. The quotient is 3 with no remainder. From above, there is already 1 pulse in the scaler, so output pulses will be obtained on the 2nd, 5th, and 8th input pulses, giving the correct quotient, 3. If it is desired to divide 10 by 3, the quotient is $3\frac{1}{3}$, which rounds off to 3. Output pulses will again be obtained on the 2nd, 5th, and 8th input pulse, giving the correct quotient, 3. If it is desired to divide 11 by 3, the quotient is $3\frac{2}{3}$, which rounds off to 4. Output pulses will be obtained on the 2nd, 5th, 8th, and 11th input pulse, giving the required quotient, 4.

If the divisor is 4 or 5, 2 presetting pulses must be fed into the scaler. If the divisor is 6 or 7, 3 presetting pulses are required. In general, as the divisor increases, one presetting pulse must be introduced into the scaler for every *other* increase in the divisor, beginning with the divisor 2.

These presetting pulses can be introduced into the scaler *only after* the control relays (or flip-flops) have registered the scaling ratio. For, if the divisor (or scale ratio) increases as the dividend increases (as would be the case, say, in averaging), and if the presetting pulses are simultaneously fed into the scaler, a false value of presetting would result, due to the continually changing operating sequences of the scaler's flip-flops. However, the presetting pulses can be fed into the dividend register with the same effect as they would have in the scaler. It is not difficult to do this. The pulses which are to be fed into the control circuit (i.e., those which determine the scaling ratio) can be fed simultaneously into another flip-flop, and the output of this flip-flop fed into the dividend storage register. The conditions for rounding off will then obtain: an additional pulse will be added for every other increase in the scaling ratio, beginning with the ratio 2. (See Fig. 8.)

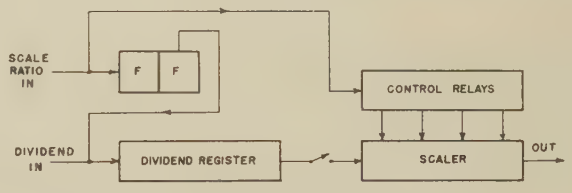


Fig. 8—A scaling circuit with provision for round-off.

Second Case

If it is desired to carry out the division to one (or more) decimal places, this can be accomplished by multiplying the dividend by 10 (or 100, 1,000, etc.). The multiplication itself can be accomplished by feeding 10 pulses into the dividend register for every digit in the units place, 100 pulses for every digit in the tens place, 1,000 for every digit in the hundreds place, etc. The rounding off of the first decimal place is accomplished in the same way as above: by feeding presetting pulses into the dividend register. Note, however, that the required number of presetting pulses remains the same as in the first case: it is not multiplied by 10.

Consider, for example, 11 divided by 3. The required quotient is $3.6\frac{2}{3}$, which rounds off to 3.7. Multiplying the dividend by 10, the problem becomes 110 divided by 3. There is 1 presetting pulse added, which means that 111 pulses are fed into the scaler, which is set to a scaling ratio of 3. Output pulses are obtained on the 2nd, 5th, 8th, 11th, etc. input pulse of the original 110 pulses. One extra pulse is added to this total of input pulses. The total number of output pulses will be 37, which represents the quotient 3.7.

In the foregoing, division was used as the simplest example. The principle applies to other functions where this kind of "automatic" interpretation is permissible. A variable scaler is not generally practical as a dividing element in a computer, because as a serial-operating device it imposes serious limitations on the speed of computation. Still, there are cases where such a scaler might replace more complex dividing circuitry, as, for example, when the dividends are relatively small, where maximum speed is not essential, or when a large number of pulse groups is to be divided by a constant number.

It must be remembered that carrying the quotient to one or more decimal places increases the time required for division by a factor of 10^n, where n is the number of decimal places required in the quotient.

Conclusion

The possibility of varying the sequence of operation of binary flip-flop elements has been illustrated in terms of a scaler of variable scaling ratio. This illustration was chosen mainly because it was the application made by the author, but also because it seems the most practical use of this feature. But applications involving some form of scaling do not exhaust the possibilities; for, by including supplementary gates (controlled by the scaler elements) and additional feedback paths, virtually any desired sequence can be obtained. A circuit could be designed to convert a series of pulses into a bi-quinary or modified bi-quinary code, or into a reflected binary code—though the usefulness of this last might well be questioned. The scaler illustrates the general principle.

Finally, it might be noted that this circuit is less complicated, and requires fewer components than the usual feed-back method of obtaining a fixed decade scaler. A disadvantage in some cases is that the intermediate states of the counter do not follow the usual "simple" binary code.

Correspondence

This section, new with this issue, is for brief reports on new ideas in the computer field, comments of timely interest, or comments on recent papers in the *Transactions*. Communications should be limited to 500 words in length. The delay between submission of the communication and its publication will be held to a minimum. Authors with material appropriate for the section are invited to send two copies to the editor.

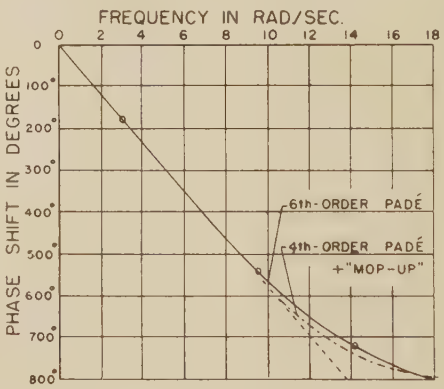
Time-Delay Circuits

The papers by Morrill[1] and Cunningham[2] on time-delay circuits suggest that the authors were unaware of work done by communications engineers[3–8] on transfer functions of the type discussed. The realization envisaged is different, of course, but the pole-locations (up to order 9)[7] and other properties may be of interest.

Cunningham's approach, that of producing what I have called "maximally-flat" delay, does in fact give precisely the same series of transfer functions as that produced by the particular Padé approximants used by Morrill. I don't know if this has been stated in print before: it is obvious when transfer functions are expressed in comparable forms.

Incidentally, something must have gone wrong in the calculation of the sixth-order curve in Morrill's Fig. 5. The numerical value of the slope of the approximate curve decreases monotonically with frequency and hence the approximate curve always lies above the ideal straight line. The sketch shows a recalculated sixth-order curve; the fourth-order plus mop-up still wins.

It is possible to realize any all-pass transfer function by a method which avoids factorization of the polynomials concerned, and hence greatly simplifies the design calculations. I am not sufficiently familiar with analog computers to say whether the resulting circuit is practicable, but the method may be of interest.



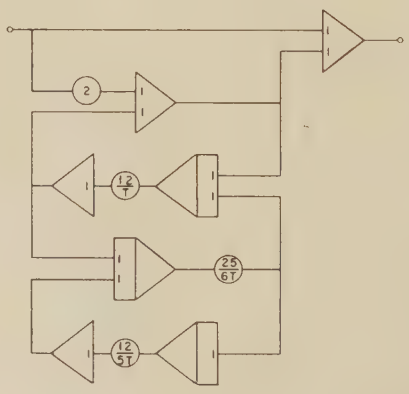


Fig. 1

The third-order maximally-flat-delay transfer function will be used for illustration. This function is

$$= -\frac{-x^3 + 12x^2 - 60x + 120}{x^3 + 12x^2 + 60x + 120}$$

where $x = sT$,

$$= -1 + \frac{-2}{1 + G}$$

where

$$G = \frac{12x^2 + 120}{x^3 + 60x}.$$

G may be expanded in a continued fraction by the usual numerical method.

$$G = \cfrac{1}{\cfrac{x}{12} + \cfrac{1}{\cfrac{6x}{25} + \cfrac{1}{\cfrac{5x}{12}}}} = \cfrac{\cfrac{12}{x}}{1 + \left\{ \cfrac{\cfrac{12}{x}\,\cfrac{25}{6x}}{1 + \cfrac{25}{6x}\,\cfrac{12}{5x}} \right\}}$$

which can be realized as a feedback circuit with feedback within feedback. The resulting circuit is given in Fig. 1.

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[1] C. D. Morrill, "A sub-audio time delay circuit," *Trans. IRE*, vol. EC-3, pp. 45–49; June, 1954.
[2] W. J. Cunningham, "Time-delay networks for an analog computer," *Trans. IRE*, vol. EC-3, pp. 16–18; December, 1954.
[3] Kiyasu-Zen'iti, "On a design method for delay networks," *Jour. Inst. Elec. Commun. Engrs.* (Japan); August, 1943.
[4] J. Laplume, "Sur la reduction de phase dans les amplificateurs a circuits decales," *Comptes Rend. Acad. Sci.* (France), vol. 227, p. 1213; December, 1948.
[5] W. E. Thomson, "Delay networks having maximally flat frequency characteristics," *Proc. IEE*, vol. 96, pt. III, pp. 487; November, 1949.
[6] J. Laplume, "Amplificateurs moyenne frequence a distortion de phase reduite," *L'Onde Electrique* (France), vol. 31, pp. 357; August, 1951.
[7] W. E. Thomson, "Networks with maximally flat delay," *Wireless Eng.*, vol. 29, pp. 256; October, 1952.
[8] L. Storch, "Synthesis of constant-time-delay networks using Bessel polynomials," Proc. IRE, vol. 42, pp. 1666–1675; November, 1954.

Contributors

R. M. Brown (M'53) was born in Cambridge, Mass., on May 17, 1924. He received his A.B. degree in electronic physics and his Ph.D. degree in physics from Harvard University in 1944 and 1949, respectively. Since 1949 he has been assistant professor of physics at the State College of Washington, Pullman, Wash. During 1952–54 he was on leave as research assistant professor at the Control Systems Laboratory at the University of Illinois.

He is a member of the American Physical Society, Sigma Xi, and the Association for Computing Machinery.

❖

W. H. Dunn was born November 23, 1928, in Passaic, N. J. He received the degrees of Mechanical Engineer in 1950 and M.S. in electrical engineering in 1952 from the Stevens Institute of Technology, where he was an instructor in the department of electrical engineering. From 1952 to 1953 he was employed as a systems engineer at the Union Switch and Signal Division of Westinghouse Air Brake Co., where he was engaged in the logical design of railroad signaling circuits.

Since joining the staff of the research division of the Moore School of Electrical Engineering, University of Pennsylvania, he has been engaged in the logical design of an electronic digital computer, and in transistor circuit design for an electronic dial telephone switching system.

❖

C. Eldert was born November 7, 1926, in Brooklyn, N. Y. He received the B.S. in E.E. from Washington University, St. Louis, in 1951. The same year he began work on his M.S. in E.E. as a member of the research division of the Moore School of Electrical Engineering, University of Pennsylvania. Since then he has been engaged in the logical design of electronic digital computers, applications of digital computers to problems in optical lens design, and abstract network theory applications to communications nets.

Mr. Eldert is a member of Sigma Xi and the Association for Computing Machinery.

❖

H. J. Gray, Jr. (S'45–A'46) was born in St. Louis, Mo., on June 24, 1924. He entered Lehigh University in 1941 and was sent two years later to the University of Pennsylvania under the Navy V-12 program, where he received the degree of B.S. in electrical engineering in 1944. After commissioning as an Ensign, he studied Navy radio and radar at Bowdoin College and the Massachusetts Institute of Technology, subsequently serving on active duty in the Pacific until 1946.

Dr. Gray received the M.S. in 1947, and the Ph.D. in 1953 from the University of Pennsylvania, where he was engaged in teaching electromagnetic field theory and work on digital and pulse techniques. Since 1954 he has been engaged in advanced development work at Remington Rand, Eckert-Mauchly Division. He is also an assistant professor of electrical engineering at the University of Pennsylvania.

He is a member of the Tau Beta Pi, Eta Kappa Nu, and Sigma Xi.

❖

P. V. Levonian (A'52) was born May 16, 1928, in Philadelphia, Pa. He received the B.S. in electrical engineering in 1949 from the Drexel Institute of Technology, and the M.S. degree in electrical engineering in 1953 from the University of Pennsylvania.

From 1949 to 1953 he was a member of the research division of the Moore School of Electrical Engineering, University of Pennsylvania, where he was engaged in the logical and circuit design of electronic digital computers. During 1953–1954 Mr. Levonian acted as technical supervisor of a government computer installation in Washington, D. C. He returned to the Moore School for the latter part of 1954 to contribute to the logical design of telephone switching systems, and at present is a member of the U. S. Navy.

Mr. Levonian is a member of Phi Kappa Phi, Tau Beta Pi, and Eta Kappa Nu.

❖

D. B. Murray, *S.J.* was born in Brooklyn, N. Y., on June 27, 1922. He attended Georgetown University for three years, leaving to become a member of the Jesuit Order. Following a two-year Novitiate, he studied Latin, Greek, and English Classics, and then majored in philosophy for three years with a physics minor, studying during the summers for the M.A. in education. He received the B.A. in 1947, and then the Ph.L. in 1948.

Father Murray taught physics and mathematics from 1948 to 1951 at Gonzaga High School in Washington, D. C., and from 1951 to 1955 studied Dogmatic and Pastoral Theology. He will now complete his course for the M.A. in education, and continue studies for the M.S. in physics.

❖

Morris Rubinoff (A'50) was born in Toronto, Canada, on August 20, 1917. He attended the University of Toronto, where he received the B.A., M.A., and Ph.D. degrees in 1941, 1942, and 1946, respectively. During World War II he participated in proximity fuse research at the University of Toronto and in England.

In 1946, Dr. Rubinoff joined the staff of Harvard University, as instructor in physics and Fellow in Applied Science at the Computation Laboratory. From 1948 to 1950 he assisted in the design of the Institute for Advanced Study electronic digital computer. In 1950 he transferred to the University of Pennsylvania, where he is an associate professor of electrical engineering, engaged in research on digital real-time simulation and telephone switching.

Dr. Rubinoff is a member of the American Physical Society, the AIEE, and Sigma Xi.

❖

Joseph Tompkins (S'52–A'53) was born in Philadelphia, Pa., on August 9, 1930. While studying electrical engineering at the Drexel Institute of Technology, he worked at the Philco Corp. on airborne radar projects in conjunction with Drexel's cooperative education program.

Upon receiving his B.S. degree in electrical engineering from Drexel in 1953, Mr. Tompkins joined the research staff of the Moore School of Electrical Engineering, University of Pennsylvania. There he is an assistant instructor, and is both engaged in graduate studies and participating in digital computer research.

❖

L. B. Wadel (S'45–A'47–M'51) was born in Dallas, Texas, on August 8, 1927. In 1946 he received the B.S. degree in electrical engineering from the Massachusetts Institute of Technology. He was concerned with the systems design of special-purpose electromechanical analog computers for airborne military application at the Norden Laboratories Corp. from 1947–1948.

Since 1948 Mr. Wadel has been with the engineering department of Chance Vought Aircraft, Inc., working in the fields of electronic analog computation and automatic flight control. He is in charge of the Chance Vought analog computer installation.

Mr. Wadel is a member of Tau Beta Pi and the Association for Computing Machinery, and an associate member of Sigma Xi and the AIEE.

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A. W. Wortham was born in Athens, Texas, on January 18, 1927. He attended East Texas State Teachers College, from which he was graduated with a B.A. degree in mathematics. He attended Oklahoma A. and M. College, receiving an M.S. degree in mathematics and a Ph.D. degree in mathematical statistics.

Since 1951, he has been employed by Chance Vought Aircraft as a mathematician and statistician. Prior to that time, while attending graduate school he served as a research assistant, graduate fellow, instructor, and statistical consultant.

Dr. Wortham is a member of Sigma Xi, the American Statistical Association, the Institute of Mathematical Statistics, American Mathematical Society, Mathematical Association of America, and the American Society for Quality Control.

PGEC News

Sectional Activities

The increasing popularity of symposia was again demonstrated by the joint study group sponsored during February and March by the New York Chapter and the local Basic Science Division of the AIEE. More than 300 registrants attended the six sessions on the role of "Digital Computers in Control Systems." The Dallas-Fort Worth Chapter is planning a National Simulation Conference.

With the approval of the Baltimore Chapter and the formation of Pittsburgh Chapter, the PGEC continues to grow; with 13 chapters and more than 2,900 paid members. Distribution of members by chapters (as of January 1, 1955) is as follows:

Akron	26
Albuquerque-Los Alamos	18
Baltimore	45
Boston	223
Chicago	72
Dallas-Fort Worth	28
Detroit	76
Los Angeles	398
New York	361
Philadelphia	270
Pittsburgh	29
San Francisco	123
Washington, D. C.	166

The other members are distributed throughout this country and Canada, and there are seven members in Israel, one in London, and one in Buenos Aires.

PGEC Elections

The new officers and administrative committee members for the 1955–1956 term are as follows:

Jean H. Felker, *Chairman*
Jerre D. Noe, *Vice-Chairman*
David R. Brown
Louis D. Wadel
Ragnar Thorensen
William H. Burkhart
John M. Broomall

Western Computer Conference

Papers on all phases of the computer field to be presented at the 1956 Western Computer Conference, sponsored jointly by the AIEE, IRE and ACM, to be held in San Francisco February 8, 9, 10, 1956, should be submitted in abstract to Byron J. Bennett, Chairman, Technical Program Committee, Stanford Research Institute, Stanford, Calif.

National Simulation Conference

The Dallas-Fort Worth Chapter of the Institute of Radio Engineers Professional Group on Electronic Computers (PGEC) will sponsor a National Simulation Conference in Dallas, Texas. The Conference will be held on January 19–21, 1956.

The Conference will be devoted to simulation and associated computing techniques, and will include topics on (1) general simulation (mathematical, physical, logistic, etc.); (2) advances in computer design, techniques, and applications; and (3) methods of determining and improving the accuracy of analog solutions.

Although it is expected that most of the papers will deal with analog computers, papers on the use of digital computers in simulation are strongly encouraged.

Prospective speakers should submit, by September 10, 1955, a 100-word abstract in duplicate together with either a 500-word summary or the complete paper itself to:

Mr. J. R. Forester
2104 Huntington
Arlington, Texas.

It is planned to publish proceedings of the Conference.

Further information regarding the Conference can be obtained from Mr. Forester.

Stanley B. Disson
News Editor
Burroughs Research Center
Paoli, Pa.

Reviews of Current Literature

It is the intention of this section to review articles that have been published since January 1, 1953, and to publish eventually reviews of all books pertaining to the computer field. Authors can be of considerable assistance in this review process by sending two reprints of their articles to H. D. Huskey, Department of Electrical Engineering, University of California, Berkeley, California. The editors wish to express their gratitude to the reviewers who, through their efforts, make this section possible.

H. D. Huskey, Editor

GENERAL

55-38

Ears for Computers—Edward E. David, Jr. (*Scientific Amer.*, vol. 192, pp. 92–98; February, 1955.) A description of an experimental computer which can recognize some elements of speech, can discriminate between the spoken numbers from zero to nine and can translate a code number into a command signal. Audrey (which stands for Automatic Digit Recognizer) can "hear" sixteen of the forty basic sounds in English. A sound spectrograph dissects the speech into twelve frequency bands and the relative amounts of energy in each band is compared with stored patterns. The machine selects the nearest match. The machine makes few mistakes when its two designers speak to her but she responds incorrectly about ten to thirty per cent of the time to other males. Audrey represents a first step toward a voice-typewriter which would automatically translate the spoken into the written word.

J. A. Fingerett

55-39

A Survey of Magnetic Recording—S. J. Begun. (*Elec. Eng.*, vol. 73, pp. 1115–1118; December, 1954.) The author presents a relatively brief statement of the present state of the art in magnetic recording. Audio, video, and pulse recording are considered. Recording media and magnetic heads are discussed.

Harry T. Larson

55-40

Information Theory and Man-Machine Systems—Gilbert K. Krulee. (*Jour. Operations Res. Soc. of Amer.*, vol. 2, pp. 320–328; August, 1954.) The article relates a series of interesting experiments performed to test the information handling capabilities of humans. The experiments involve the visual recognition of symbols or the selection of cards according to symbols. The general nature of the findings can be summarized as follows: 1. The human spends more time in handling information, if there is more information to handle; 2. This relationship between amount of information and time is not linear; 3. Anticipatory information aids the human in making a selection; 4. Irrelevant information is easiest to eliminate, if it is readily fitted into a single category. There is indication in the article that considerable theoretical analysis is back of these experiments, but such theory and derivations are kept out of the essay form of the paper. Essentially, one table is the only significant quantitative information supplied. The symbols in this table are unexplained, so that the reader finds himself the subject of the type of experiments the paper describes.

John M. Salzer

55-41

Some Mathematical Aspects of Switching—Franz Hohn. (*Amer. Math. Monthly*, vol. 62, pp. 75–90; February, 1955.) This article apparently is intended to stimulate interest among mathematicians in the abstract problems of switching theory, and admittedly contains no new theoretical developments. Relays are introduced as the simplest representation of the two-state switching elements being used, and correspondence between the schematic and algebraic representations of their two-terminal switching circuits is established. Some brief examples of simplification by algebraic manipulation, development of the two canonical forms, a short discussion of the combinatorial circuits, and an outline of some of the important mathematical problems associated with economical circuit design serve to fill out the body of the article. Except for the sixteen-item bibliography, which includes recent works on sequential circuits and on such as group-theory, lattice-theory and geometrical approaches to the algebraic problems, the article would seem to add little to the computer engineer's reference list . . . but the reviewer sincerely hopes that it succeeds in stimulating the right mathematicians.

Douglas C. Engelbart

681.142 55-42

Theory of Logical Nets—Arthur W. Burks and Jesse B. Wright. (Proc. IRE, vol. 41, pp. 1357–1365; October, 1953.) This mathematical paper attempts to place on a more formal basis certain aspects of logical nets and their application to digital computing circuits. Throughout a mathematically rigorous approach is followed. Two primitive elements are defined and introduced: a *stroke element* to represent circuit components which appear as logical elements, and a *delay element* to represent circuit components which appear as storage elements. The concepts of a *well-behaved net*, a *deterministic net*, and a *well-formed net* are introduced and precisely defined. A suitable set of equations to describe the behavior of each type of net is also introduced. Fourteen theorems relating to these types of nets are proved. Finally the possibility of realizing well-formed nets by means of digital computing circuits is discussed and an additional six theorems are proved.

Willis H. Ware

ANALOG COMPONENT RESEARCH

681.142:621.375.2.024 55-43

Time-Shared Amplifier Stabilizes Computers—D. W. Slaughter. (*Electronics*, vol. 27, pp. 188–190; April, 1954.) This article describes a dc amplifier used to stabilize operational amplifiers in analog computers. The amplifier may be time-shared with thirty operational amplifiers. Details of amplifier, output filter and switching circuits design are presented and interaction between operational amplifiers discussed. The author concludes the article by giving details of system performance.

Norman F. Loretz

681.142:621.385.012 55-44

Making Use of Curved Characteristics for the Higher Types of Calculation in Electronic Computers—H. Harmuth. (*Acta Phys. austriaca*, vol. 8, pp. 332–337; July, 1954.) Where errors up to a few per cent are permissible, deliberate use can be made of the curvature of tube characteristics in analog computers. Circuits for multiplying, dividing, squaring and obtaining square roots are discussed.

Courtesy of Proc. IRE and *Wireless Engineer*

681.142 55-45

A Time-Sharing Analog Multiplier—H. Freeman and E. Parsons. (*Trans. IRE*, vol. EC-3, no. 1, pp. 11–17; March, 1954.) The circuit is based on the same principle as that of Broomall and Riebman (see Proc. IRE, abstract 2546 of 1952). Accuracy to within 0.2 per cent is achieved for a range of input voltages from 0 to 210 v when the comparator voltage lies between 0 and 75 v, depending on the circuit arrangements. 400 multiplications per second were made, indicating the suitability of the circuit for time-sharing techniques, but higher rates of operation seem possible.

Courtesy of Proc. IRE and *Wireless Engineer*

681.142 55-46

Amplitude Comparator for Computing Purposes—T. Z. Aleksić. [*Bull. Inst. Nuclear Sci.* (*Belgrade*), vol. 4, pp. 13–19; June, 1954. In English.] A simple circuit is described which gives uniform output pulses

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—The Editor

for a large range of input-signal derivatives. Low transformer output impedance is provided. Measures are indicated for ensuring stability when the signals are slowly varying.

Courtesy of PROC. IRE and *Wireless Engineer*

ANALOG EQUIPMENT

681.142 55-47

A New German Differential Analyzer for Differential Equations—A. Walther. (*Z. Ver Dtsch. Ing.*, vol. 96, pp. 755–758; August 1, 1954.) A mechanical instrument built for the Institute of Applied Mathematics, University of Bonn, and comprising 8 integrators.

Courtesy of PROC. IRE and *Wireless Engineer*

UTILIZATION OF ANALOG EQUIPMENT

681.142 55-48

Some Applications of Elements with Discontinuous Operation in Analogue Computation—D. M. Mitrovic. [*Bull. Inst. Nuclear Sci. (Belgrade)*, vol. 4, pp. 1–11; June, 1954. In French.] See "A Nonlinear Servomechanism with Several Independent Variables"—D. Mitrovic. [Compt. Rend. Acad. Sci. (Paris), vol. 237, pp. 1209–1211; November 16, 1953.] The field of application of the differential analyzer is enlarged by incorporating amplitude comparators and electronic switches. Solution of particular differential equations is discussed.

Courtesy of PROC. IRE and *Wireless Engineer*

55-49

Equipment Reliability as Applied to Analogue Computers—H. Jacobs, Jr. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 21–26; January, 1954.) A general description of the M.I.T. Flight Simulator is followed by a discussion of its component maintenance program. Listed are seven checks found valuable in the maintenance checking of the amplifiers. Satisfaction of all seven indicates high probability of serviceability for entire maintenance cycle. Rough criteria are developed for optimum maintenance cycle length to give minimum total cost/month (cost of preventive maintenance plus cost in machine hours lost in locating trouble). Plot of cost vs cycle length shows a minimum at about 4 months for Ar-10 amplifier. Author emphasizes importance of keeping records of each component. Types of records kept at M.I.T. are discussed.

W. W. Soroka

DIGITAL COMPONENT RESEARCH

55-50

Flip-Flop Counter Has Expanded Range—Howard Beckwith. (*Electronics*, vol. 28; pp. 149–151; January, 1955.) This article describes a flip-flop counter which may have up to six stable states without the use of feedback. An N state counter requires N tubes with only one tube conducting at any time. For values of N less than seven the number of tubes required is equal to or less than the number used in conventional counters. As N increases, less reliable operation is experienced because of interaction between grid to plate coupling networks. However, this interaction can be eliminated by using a crystal diode matrix in the flip-flop cross-coupling networks. The advantages of this type counter are fewer tubes, elimination of feedback matrix and sequential output without using a matrix. In the article the author derives a set of design equations.

Norman F. Loretz

681.142 55-51

An Operational-Digital Feedback Divider—M. A. Meyer, B. M. Gordon, and R. N. Nicola. (*Trans. IRE*, vol. EC-3, no. 1, pp. 17–20; March, 1954.) In this divider the input pulses operate directly on the output, the circuit forming a closed feedback loop in which the desired quotient corresponds to the only possible steady state. The accuracy of the system can be selected by using the appropriate number of significant digits from the eleven available.

Courtesy of PROC. IRE and *Wireless Engineer*

55-52

Magnetic Core Selection System—S. Guterman and R. D. Kodis. (*Convention Record of the IRE, 1954 Nat. Conv.*, Part 4, pp. 116–123; 1954.) Selection of one magnetic drum head out of many for recording and playback is accomplished by means of magnetic cores. The recording selection system utilizes a pair of cores with rectangular hysteresis loops and two diodes per head. The usual binary inhibiting configuration selects the pair and the polarity of write-in. Good signal-to-noise and reliability are reported in recording systems. The playback selection system utilizes saturable cores with appreciable incremental permeability at remanence arranged by pairs in a classical pyramid structure. Promising results with the playback selection system are reported but a desire for better materials and layouts is expressed.

Jan Rajchman

55-53

Considerations for the Selection of Magnetic Core Materials for Digital Computer Elements—O. J. Van Sant, Jr. (*Convention Record of the IRE 1954 Nat. Conv.*, Part 4, pp. 109–115; 1954.) Magnetic field strength, signal-to-noise ratio, and power consumption may be plotted against the inverse switching time to compare different magnetic materials for application in magnetic-core memories. The three curves are determined by a series of measurements on a single core. The magnetic field strength is the amplitude of an applied field which switches the core under test during an interval defined as the switching time. The signal-to-noise ratio is a ratio of flux changes. A signal is defined as the flux change which takes place when the core is switched by an applied field which has been preceded by five or six half-amplitude pulses of field. Noise is defined as the largest flux change which can be produced with a half-amplitude field pulse. Power consumption is plotted as the product of magnetic field strength and the peak rate of change of the flux density when the core is switching. These curves permit an approximate comparison of different materials for operation at a given switching time, but the author cautions that only cores of the same size or proportions should be compared. The discussion is qualitative and not related to specific materials.

David R. Brown

55-54

An Alpha Plotter for Point-Contact Transistors—T. P. Sylvan. (*Elec. Eng.*, vol. 73, pp. 1094–1098; December, 1954.) This paper describes a test set for plotting alpha, the ac short-circuit gain, versus emitter current on an oscilloscope. Such a plot is useful in large signal switching circuits because alpha governs the negative resistance characteristic, which determines the speed at which the transistor switches from "off" to "on" and the degree to which it is "off" or "on." The test set consists of a 33 cps oscillator for providing emitter "bias" and horizontal sweep for the oscilloscope, a 100 kc transistorized oscillator providing the "signal" emitter current, a high pass filter, and a transistorized 100 kc amplifier. Alpha is measured as the ratio of the magnitude of the 100 kc current component at the collector to the magnitude of the 100 kc current component at the emitter. A complete circuit diagram and parts list is included.

Harry T. Larson

55-55

Testing Point-Contact Transistors for Pulse Applications—R. L. Wooley. (*Elec. Eng.*, vol. 73, pp. 981–987; November, 1954.) When point-contact transistors are used in pulse or switching circuits, their nonlinear large-signal characteristics, rather than their linear small-signal characteristics, are of primary importance. This article describes methods of test for large-signal pulse applications. Typical input and output static characteristics are divided into three major regions. A set of dc, dynamic, and static parameters are chosen that describe pertinent behavior of transistor in each of the three regions. Ways of measuring these parameters are given, including test circuit diagrams. A variety of testing difficulties and appropriate precautions are discussed. Conclusions are drawn on measurements for determining proper application of transistors to large-signal pulse circuits.

Harry T. Larson

55-56

A Point-Contact Transistor Test Set—R. S. Hill. (*Elec. Eng.*, vol. 74, pp. 59–62; January, 1955.) This article describes a point-contact transistor test set which measures the important performance characteristics of point-contact transistors intended for use in large-signal applications of the pulse and switching circuit type. The device makes seven dc measurements, presented on meters. With aid of an oscilloscope and camera, the V_c vs I_c family with I_E as parameter can be recorded. With aid of a pulse generator and oscilloscope, dynamic measurements on rise time, fall time, ohmic delay, and storage time can be made. The body of this article is devoted to operating instructions and circuit diagrams for tester.

Harry T. Larson

681.142:621.392.5 55-57

Electrical Delay Lines for Digital Computer Applications—J. R. Anderson. (*Trans.*

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—The Editor

IRE, vol. EC-2, no. 2, pp. 5–13; June, 1953.) The maximum storage capacity of commercially available lumped-parameter and distributed-parameter delay lines is about 23 and 15 pulses respectively, regardless of total delay time. An analysis indicates that dissipation in inductive elements is the chief limiting factor. Insertion loss can be reduced and storage capacity increased to about 32 pulses by using as inductive elements low-permeability, high-*Q*, Ni-Zn ferrites around straight single conductors. The design of such units is described.

Courtesy of PROC. IRE
and *Wireless Engineer*

681.142:621.385.832 55-58

Automatic Beam Current Stabilization for Williams Tube Memories—R. J. Klein. (*Trans. IRE*, vol. EC-2, no. 4, pp. 8–11; December, 1953.) One of the storage points in the memory tube is used as a test point. At regular intervals this is cleared and recharged, and the output is sampled, the beam current being adjusted to keep the sampled output at a constant level. The whole operation takes 40 microseconds to complete. Circuit details are given.

Courtesy of PROC. IRE
and *Wireless Engineer*

55-59

Quarterly Report No. 5, Second Series—J. R. Bowman, F. A. Schwertz, et al. (*Quart. Rept. Computer Components Fellowship Mellon Inst.*, 82 pp.; October 1, 1954, to December 31, 1954.) The report contains two main parts. Part I is entitled "Techniques for Circuit Fabrication" and has to do with various methods for obtaining printed wiring boards and printed passive components. The techniques include xerography, xeroprinting, vacuum depositing and spraying. Of particular interest is an account of some experiments ultimately aimed at obtaining a simple circuit containing resistors and capacitors which will be operable in the range 200 degrees to 300 degrees C. Part II has to do with electro-optical devices, and, in particular, with electroluminescent light sources and an electro-optical bit store comprising a photocathode and a phosphoranode within the same evacuated space.

F. A. Schwertz

DIGITAL EQUIPMENT

55-60

Reliability Experience on the OARAC—Robert W. House. (*Proc. Eastern Conf., Joint IRE-AIEE-ACM, December 8–10, 1953, Washington, D. C.*, pp. 43–44; 1954.) This paper presents a general resume of the operating experience with the OARAC machine. The OARAC is a general purpose, coded decimal, medium speed, magnetic drum machine. It has a word length of eleven decimal digits and a storage of 10,000 words. The input-output medium is magnetic tape operating at 50 inches per second and 17 pulses per inch. To date, the output operation is felt to be more reliable than the input, and almost no difficulty has been encountered with head misalignment, or tape imperfections. This machine was delivered in February, 1953, to the Wright Air Development Center and has been operated most of the time on a 3-shift basis. Until latter October, the largest percentage of of errors was caused by the memory, but engineering redesign has now remedied this difficulty. The arithmetic and control units contain many built-in checks. Among these are checks for division by zero; excessive length of sum or product; incorrect drum addresses; the appearance of forbidden combinations, etc. The original 1N52 germanium diode has been recently changed to the 1N63 germanium diode. This, plus the addition of air conditioning including humidity control, and plus a reduction in back voltage on the diodes, has resulted in a diode failure rate of 10 diodes per 120-hour week. The principal tube types are the 12BH7 and the 2C51. The 12BH7 is estimated to have a life of 12,000 hours, the 2C51 a life in excess of this.

Willis H. Ware

55-61

Basic Circuitry of the MIDAC and MIDSAC—J. E. De Turk, H. L. Garner, J. Kaufman, H. W. Bethel, and R. E. Hock. (*University of Michigan Engineering Research Institute Report No. 1947–2 T*, 112 pp. May, 1954.) This report describes the electronic computing circuit packages which were developed at the Willow Run Research Center to serve as the principal building blocks for both the MIDAC and MIDSAC. The computing circuits are pulse circuits which operate at a one megacycle pulse repetition rate. This work was based on existing techniques developed by the National Bureau of Standards for use in the SEAC, and with whom a co-operative development program was initiated. The report is divided into four parts, the major division (Part I) being given to a description of the function, operation, and design of the packaged circuitry. Part II is a description of several functional units assembled from the basic packages, and Part III describes a serial-binary arithmetic unit composed of functional units from Part II. Part IV describes constructional features of the packages and their mountings. Included are considerable detail on the basic packages, examples of some design calculations, suggested improvements in construction and fabrication techniques and illustrations of design possibilities, including an etched-circuit package.

A. S. Hoagland

681.142 55-62

System Organization of the DYSEAC—A. L. Leiner and S. N. Alexander. (*Trans. IRE*, vol. EC-3, no. 1, pp. 1–10; March, 1954.) DYSEAC is a general-purpose high-speed digital computer incorporating the following special facilities: (a) external-transfer operations concurrent with internal computing, such transfers referring directly to any area of the internal storage system; (b) adjustment of speed of internal program so that it proceeds in step with the external program; (c) interruption of a program for interpolation of new orders.

Courtesy of PROC. IRE
and *Wireless Engineer*

55-63

Design Features of Remington Rand Speed Tally—J. L. Hill. (*Trends in Computers: Automatic Control and Data Processing, Proc. Western Computer Conf., Joint AIEE-IRE-ACM, February 11–12, 1954, Los Angeles, Calif.*, pp. 155–162; April, 1954.) The Remington Rand Speed Tally was developed to handle the tallying operations of the John Plain Company. The equipment was designed to handle tallies for 13,000 items at a rate of 74,000 tallies per day. For each of the 13,000 items three tally totals are provided so that tallies can be kept of orders, sales and cancellations. Thus, the equipment provides for a total of 39,000 tallies. Input is via a keyboard. A five-decimal catalog number specifies the item, a "one of three" designation of the category and a two-digit quantity are the required input information. Usable output is by way of a perforated tape reader specifying the desired items and an adding machine type printer. It is possible to print out all 13,000 totals in one category in less than three hours.

Norman F. Loretz

55-64

The IBM Magnetic Drum Calculator Type 650—F. E. Hamilton and E. C. Kubie. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 13–20; January, 1954.) A descriptive account of a decimal calculator employing the bi-quinary code for logical and arithmetic operations and the two out of five code for recording on the magnetic drum. There is a general description of the arithmetic circuits, logical layout, self-checking features, instruction code, input-output equipment and construction of the magnetic drum.

L. C. Nofrey

681.142 55-65

Lectures on Electronic Computing—L. Kosten and W. L. v. d. Poel. (*Tijdschr. ned. Radiogenoot.*, vol. 19, pp. 211–212; July, 1954.) English summaries are given of the following papers: "The History of the Electronic Computing Machine 'PTERA,' Purpose and Possibilities,"—L. Kosten; "The Functioning of the Electronic Computing Machine 'PTERA',"—W. L. v. d. Poel; "Programming for the Electronic Computing Machine 'PTERA',"—W. L. v. d. Poel; "Discussion of Programme 'A7' for the Electronic Computing Machine 'PTERA',"—L. Kosten. The complete papers are published in *P. T. T. Bedrijf*, vol. 5, pp. 116–149; 1953.

Courtesy of PROC. IRE
and *Wireless Engineer*

55-66

The IBM Type 702, An Electronic Data Processing Machine for Business—C. J. Bashe, W. Buchholz, and N. Rochester. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 149–169; October, 1954.) As the title implies, the IBM 702 is a large scale, general purpose, decimal, serial computer, designed for business applications. Its distinct feature, as compared with other scientific and business computers, is its word organization. A word may be an instruction, a number, or a statement. The word length in a scientific computer is fixed, but the word length in the IBM 702 computer is variable. The word length may be adjusted by the programmer to describe the data under consideration. The basic unit of information storage in the

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IBM 702 is a character, which may be a decimal digit, a letter of the alphabet, or a special symbol. A word can be anything from a single character to 511 characters. The internal electrostatic memory has a capacity of 10,000 characters. Each of the two electrostatic accumulators has a capacity of 511 characters. A character is composed of seven bits; one bit is used for even count redundancy checking and six bits are used for the information. A single address code of five characters is used. One character describes the operation and four characters specify the memory address of the signed characters of the operand (if it is a numerical instruction). As all the numerical data stored in the internal memory are signed numbers, the length of the number is determined by recognizing the signed zones between adjacent signed numbers. When an accumulator is used to accommodate numerical information, its length is self-adjusted according to the length of the number, whether it is directly from the internal memory or the result of computation. When the accumulator is used to accommodate nonnumerical information of known length, the length of the accumulator is set by a previous accumulator length set instruction. Once the accumulator length is set, it will receive only the fixed number of characters from the memory. The IBM 702 general characteristics, code chart, instructions as well as an example of programming on variable-length numerical data are given and discussed at length.

J. C. Chu

UTILIZATION OF DIGITAL EQUIPMENT

55-67

Running a Computer Efficiently—C. C. Gotlieb. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 124–127; July, 1954.) The Computation Centre of the University of Toronto operates FERUT, the Ferranti electronic high-speed digital computer. The problems in operating FERUT seem to be those of most computing centers with large size computers and the article is a useful summary of these, coupled with some of the means used to obtain efficient operation at the Centre. The working schedule allots twenty-one hours, of a total of 105 per week, to scheduled engineering and maintenance. Roughly seven-eighths of the remaining time is good computing time, utilized by a staff of fifteen programmers. It is not stated how many engineers are employed. An extensive library of routines is kept up-to-date by the programmers through frequent discussion meetings. Monthly supplements to the operating manual are issued. The author describes programmed checking devices, which help to minimize the difficulties of a scale 32 notation, as well as a very complex set of machine orders. Engineered aids to coders are available. One useful device, the "Development Switch," allows the computer to proceed at 1–50 normal speed, and prints a character for each operation, specifying which instruction has been obeyed. Records of machine performance must be accurately and completely kept. In addition to supplying data for cost accounting, such records are invaluable aids to maintaining successful operation. A simple but efficient method of recording machine activity is described. Despite all the record keeping the author still finds it difficult to estimate accurately the time and cost for running a problem, although the growing library of subroutines is making this easier.

Frederick Hollander

55-68

On the Demonstration of High Speed Digital Computers—Walter F. Bauer and John W. Carr, III. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 177–182; October, 1954.) The authors consider the problem of the presentation of a lucid series of routines that will be explanatory and interesting in both the mathematical and visual sense to those viewing the demonstration of a high-speed digital computer. Great emphasis is placed on the two-way communication between the computer and the audience. Emphasis is also given to the simplicity of the statement of the problem and the use of games. As an example, the article contains a demonstration routine used on the MIDAC.

David H. Jacobsohn

55-69

The IBM *701* Speedcoding System—J. W. Backus. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 4–6; January, 1954.) The article describes the IBM 701 Speedcoding System. Its advantages of reduced coding time and check-out time are described. Speedcoding is a three-address decimal floating point code and further provides for a second operation code and fourth address to facilitate logical operations. Three "B" registers provide for automatic address modification. Selected regions of a program or entire programs can be automatically recomputed for checking. Three levels of break point printing are provided under control of console switches. This feature is an important advantage for program checking. Examples are cited indicating that savings of programming time on the order of ten to one can be realized in comparison with standard machine language programming. Speedcoding operates in an interpretive mode. The interpretive program occupies most of the high-speed memory leaving approximately 700 full words for storage of data and instructions. Running time is very much greater than for a program in machine language. Blocks of data can be transferred between memory and tapes or drums by one Speedcoding instruction. All coding is decimal. Automatic input from cards and printing of results are provided. Five 701 installations are using, or plan to use Speedcoding. The system is an important contribution to the rapid and economical use of the 701.

John R. Lowe

55-70

The Generation of Pseudo-Random Numbers on a Decimal Calculator—Jack Moshman. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 88–91; April, 1954.) Moshman considers the behavior of the digits in the numnumbers r_n defined by $r_0=1$, $r_{n+1}=rr_n \pmod{10^{11}}$. The sequence $\{r_n\}$ itself has period 5×10^8 when $r=7^{13}$ and it can be generated easily on UNIVAC: in fact r_{n+1} is the content of the X-register in the P-product of r and r_n. Let $d_n=d_n(m)$ be the m-th digit in r_n, counting from the right. It is easy to verify that $\{d_n(1)\}=\{1, 7, 9, 3, 1, 7, \cdots\}$; this sequence has period 4 and is certainly not very random. However, as m increases, the period becomes larger, e.g. $\{d_n(6)\}$ has period 5,000. A battery of tests for randomness was applied in the cases $m=7$, 8, 9, 10, 11 to the first 10,000 numbers taken as a whole, and in groups of 2,000. All tests were passed satisfactorily; the sequence in the case $m=6$ appeared too random. These results, together with similar experiments on the Aberdeen and National Bureau of Standards machines, among others, indicate that this multiplicative generation of pseudo-random numbers or digits is very adequate for sampling problems on electronic computers. This method appears to be preferable to the mid-square method or the additive method.

John Todd

55-71

The Calculation of the Latent Roots and Vectors of Matrices on the Pilot Model of the A.C.E.—J. H. Wilkinson. (*Proc. Camb. Phil. Soc.*, vol. 50, part 4, pp. 536–566; October, 1954.) The Pilot A.C.E. has a very limited high-speed storage capacity and hence iterative methods, having simpler programs, are usually preferred to direct methods. This paper contains a comprehensive and critical survey of iterative methods from the viewpoint of automatic computing, and describes the methods used on the Pilot A.C.E. The theory of each method is clearly presented, and many points of practical interest are noted (such as the conditions under which matrix squaring is worth while). A feature of the A.C.E. programs is that floating point arithmetic is avoided. When the paper was written the A.C.E. had no auxiliary store, but very efficient use was made of punched cards for intermediate storage. Experience has shown that a simple iterative process with successive root removal gives surprisingly accurate results, even for matrixes of order 50.

S. Gill

55-72

The Evaluation of a Diffraction Integral—D. R. Hartree. (*Proc. Camb. Phil. Soc.*, vol. 50, part 4, pp. 567–574; October, 1954.) The author describes how he approached the computation of certain integrals on the EDSAC, using partly quadrature and partly the integration of differential equations. Some experiments on the errors in various applications of Gauss quadrature formulas produced interesting results.

S. Gill

55-73

Automatic Digital Computers in Industrial Research—R. F. Clippinger, B. Dimsdale, J. H. Levin. (*Jour. Soc. Industrial and Applied Math.*, vol. 1, pp. 1–16; September, 1953; vol. 1, pp[91–110; December, 1953; vol. 2, pp. 36–56; March, 1954; vol. 2, pp. 113–131; June, 1954; vol. 2, pp. 184–200; September, 1954.) In this sequence of articles the authors make a useful contribution toward answering the following six questions which arise in businesses concerned with industrial research, data handling or control: (1) To what extent can my

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—*The Editor*

problem be solved by digital computers? (2) Will a digital computer lower my costs and increase the range of problems I can solve? (3) Should I obtain a computer of my own or should I send my problems to a central computing laboratory? (4) How do I recognize a problem to which a digital computer could contribute? (5) How do I prepare my problem for solution on a digital computer? (6) Will a computer enable me to forge ahead of my competitors?

T. H. Southard

55-74

Public Utility Customer Accounting on the Type 650 Magnetic Drum Data Processing Machine—George F. Trexler. (*Jour. Assoc. Comp. Mach.*, vol. 1, pp. 173–176; October, 1954.) This article describes the application of the IBM 650 computer to a public utility customer's billing operation and accounting procedure. The three main operations of the accounting and billing process are: (1) Meter reading; (2) Bill calculation and preparation; (3) Accounts receivable. The use of IBM cards to carry out these accounting processes is described in detail. No engineering details, order list or computation speed of the IBM 650 are given.

J. C. Chu

BOOK REVIEWS

55-75

Automatic Digital Computation—(National Physical Laboratory. Her Majesty's Stationery Office, 296 pp.; 1954.) The International Symposium on automatic digital computers held at the National Physical Laboratory, Teddington, in March, 1953, was the third of its kind in England. These summarized reports on the discussions are based on notes taken at the time by the various reporters, checked and supplemented by reference to a magnetic tape recording of the proceedings. It has, of course, been necessary to condense the reports of the discussions in order to keep the record to a reasonable size.

Courtesy of *Electronic Engineering*

55-76

Review of Electronic Digital Computers—(American Institute of Electrical Engineers, New York, 114 pp., illus.; 1952.) Review of Electronic Digital Computers gives the most up-to-date information concerning the actual operation of large-scale digital computers which is available. It comprises the proceedings of the Second Joint Computer Conference, but each paper was written in advance by an invited author with the idea that the group of papers would form the printed symposium here presented. The objective is a picture of actual operating experience with large-scale digital computers now in operation. Considerable emphasis should be placed on the two phrases "actual operating experience" and "now in operation." The Review does not discuss machines under construction, nor does it devote space to such machines of old age as the ENIAC (six years of operating experience, hence old in a field that is moving as rapidly as this one). "Old" machines have settled down; the ENIAC, for example, continues on its 24-hour-a-day schedule and probably has long since turned out more results than all the formal computations produced in the world before its inception. The papers are outstanding in the frankness of their approach. This was a Review for people who know the difference between operating experience and hopes, expectations, propaganda, advertising, and other ephemeralities. Furthermore, the authors were available for open discussion, almost all of which is reported in the volume under review. Rather than discuss the reported practical results of the use of new machines, this review will be devoted to a few related items presented in the volume. This is because many of the frankly discussed operating troubles, defects, deficiencies, etc. mentioned are matters to be taken in stride and, in some cases known to the reviewer, have been substantially overcome in the time since the papers were prepared. But even optimistic workers in the large-scale computing devices field may be impressed by some of the figures presented by Charles R. Strang, engineer of the Douglas Aircraft Company, Inc. He describes the practical and imminent possibility of eliminating one to two million man-hours of engineering work in the design of a modern plane. He presents data showing that Douglas will shortly be spending one million dollars per year on computing with large-scale devices, not including in this figure purchase cost of the devices. Mr. Strang discusses typical problems, for example, a catapult problem. In the latter the machine analysis, used for the first time because the magnitude of the computing program involved had deterred previous attempts to apply theoretical analysis, was parallel by field tests. Mr. Strang implies that the tests showed nothing that the mathematical analysis did not correct in the design, cost several times the price of a large-scale computing machine, and we may infer (although Mr. Strang does not mention this) that the analysis had no casualty list corresponding to the one that would be inevitable in attempting to test the catapulting of a plane not operating well from a catapult. An adequate computing facility for his company would handle not a few such problems, but several hundred, a state which the author describes as "a really full-scale use of an adequate computing facility in a large engineering effort." A summary and some predictions were made by Jay W. Forrester of Massachusetts Institute of Technology. Throughout the papers the operating experiences described relate primarily to reliability. A reliability rate mentioned for mechanical relay devices, such as 35 million operations of one of the relay machines per random mistake, can be achieved by one of the modern electronic machines in 1 to 2 hours of operation. An error frequency of one in three hundred million operations is a practical achievement; an aim of one random error per billion operations is well within the realm of early realization. Practically, this comes down to requiring one of the modern machines to operate somewhere between 24 and 48 hours without a random error. Forrester goes on to say that when such reliabilities are attained, checking devices will be unnecessary. For less reliable machines, in the rank say of one random per hundred million operations, programmed checks appear adequate. Forrester points out that storage devices such as magnetic drums, acoustic lines, and cathode-ray tubes, are likely to be superseded by new devices, the investigation of which is just beginning. These may not only be better technically, but they may have the valuable property of bringing the cost per unit of performance down by at least one order of magnitude. Although "the higher speed machines are more efficient in terms of work they will perform per unit of equipment," it does not appear likely that there will be great effort to increase the speed of modern machines, chiefly because there is a feeling that speed has been achieved while many other components of computers lag. Particularly has input-output equipment been brought into question (a fact which provides the topic for the next volume of the series of which this Review is the first to be published). The volume covers a topic of prime current importance in the field in a fully adequate manner and offers much valuable information of a type not often reaching print. It is stimulating and furthermore, it is a bargain.

J. G. Brainerd

Courtesy of
The Review of Scientific Instruments

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